

# **miniMODUL-167**

## **Hardware Manual**

**Edition May 2002**

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## Preface

This miniMODUL-167 Hardware Manual describes the board's design and functions. Precise specifications for the SABC167 microcontroller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

### Declaration regarding EMV-Conformity of the PHYTEC miniMODUL-167



PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

#### **Caution:**

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the EMVG-statute only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC). Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, EMV-Statutes. Only after doing so the devices are allowed to be put into circulation.

The miniMODUL-167 is one of a series of PHYTEC nano-/micro-/miniMODULs which can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common Infineon 8- and 16-bit controllers in two ways:

- (1) as the basis for Starter Kits in which user-designed hardware can be implemented on a wrap-field around the controller and
- (2) as insert-ready, fully functional micro- and miniMODULS which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. Please contact PHYTEC for additional information.

## **1 Introduction to the miniMODUL-167**

The miniMODUL-167 is an extension of the PHYTEC miniMODUL-166. It is intended for use in memory intensive applications and the driving of a CAN bus (C167Cx). Furthermore, the module is fitted with a Real-Time Clock which, like the RAM, can be battery buffered. An additional UART is fitted on the module, in place of the second asynchronous serial interface of the C166. As well as the address and data buses, 64 free port lines are provided, including 16 analog inputs with 10-bit resolution.

The miniMODUL-167 is pre-configured and equipped with all necessary connectors required for immediate start-up (*refer to Figure 2*).

**The miniMODUL-167 offers the following features:**

- credit card-size dimensions (55 x 85 mm) achieved through modern SMD technology
- improved interference safety through multi-layer technology
- can be plugged into any electric application like a 'big chip'
- requires a single power supply of 5 V<sub>=</sub>, typ. < 200 mA
- close pin compatibility to the miniMODUL-166
- 16-bit, non-multiplexed bus mode
- 20 MHz CPU speed (100 ns / instruction cycle)
- 16 MB Address space, up to 4 MB memory on-board
- up to 2 MB SRAM on-board  
(up to 1 MB can be buffered with a battery) <sup>1</sup>
- up to 2 MB Flash memory on-board <sup>1</sup>
- on-board Flash-programming
- no dedicated programming voltage required through use of 5 V-Flash-devices
- up to 2 MB (EP)ROM on-board <sup>1</sup>
- battery buffered RTC with 256 Byte RAM
- RS-232 transceiver for two serial interfaces
- UART as a second asynchronous serial interface
- provision for operation with in-circuit emulators (ICE/connect 167-interface).

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<sup>1</sup>: For more information about different configurations see the PHYTEC product catalog

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## 1.1 Block Diagram

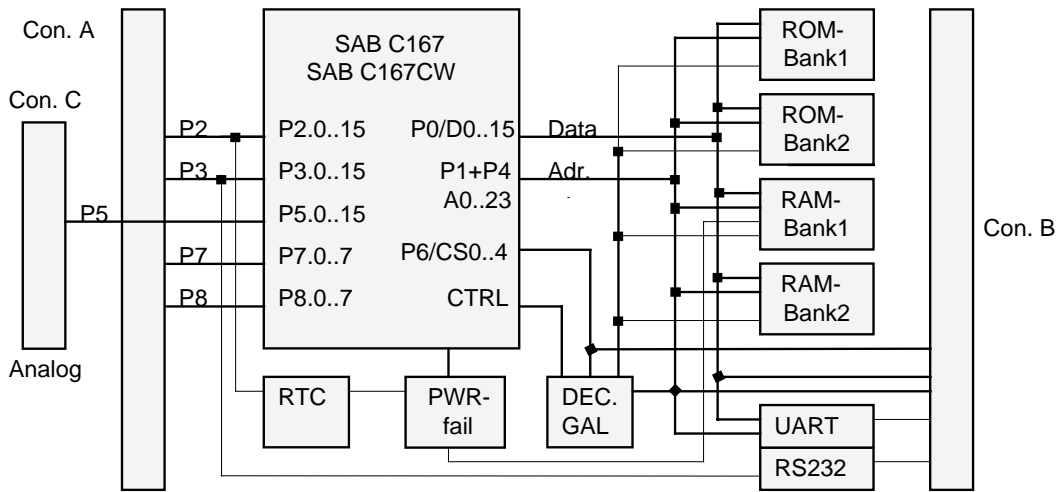


Figure 1: miniMODUL-167 Block Diagram

## 1.2 Overview of the miniMODUL-167

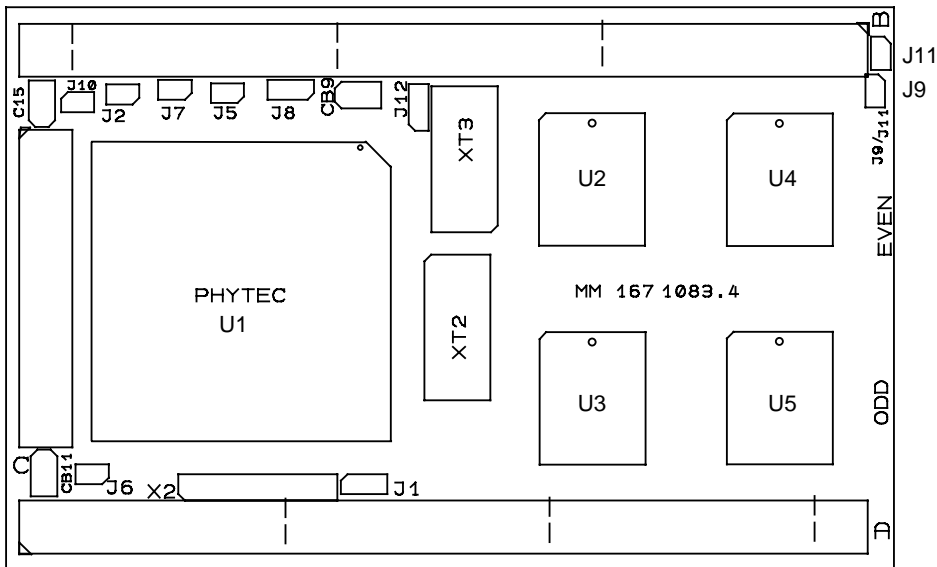


Figure 2: Overview of the miniMODUL-167 (Component Side)

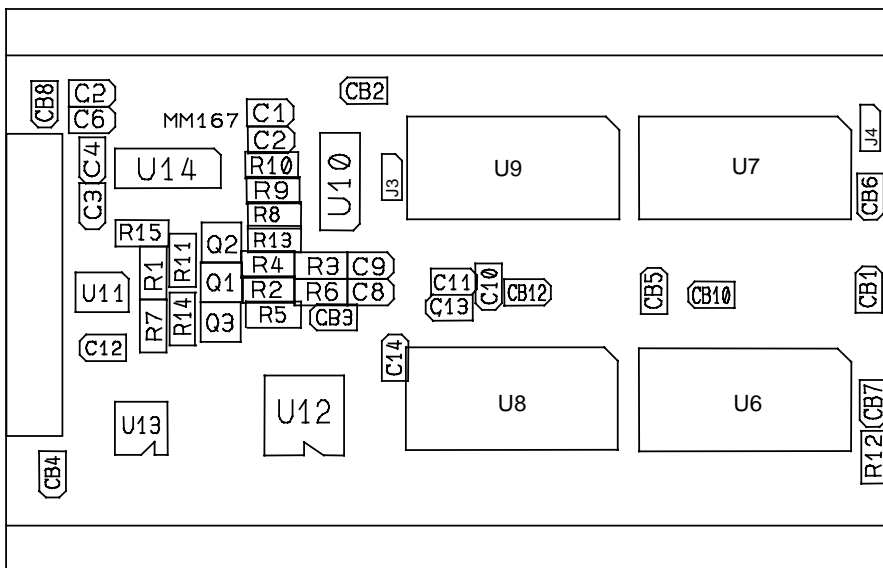


Figure 3: Overview of the miniMODUL-167 (Soldering Side)

## 2 Pin-Layout

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum input values are indicated in the corresponding controller manuals. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

**Caution:**

The miniMODUL-167 is based on CMOS technology and, hence, is particularly sensitive to power surges and ESD. Accordingly, unused inputs should be connected to Vcc or GND.

The miniMODUL-167 has three pin contact rows (A, B and C) (*refer to Figure 4*) in the form of a dual-rowed socket in a 2.54 mm grid underneath on the circuit board. All relevant signals of the C167 controller, the peripheral hardware and the power supply are connected via these pins. Terminals A and B of the module are arranged as two 64-pin connectors along the right and left edges of the module. These connectors include all digital signals with TTL levels, as well as the power supply and RS-232 interface. Contact row C is on the upper edge of the module, running perpendicularly between rows A and B. It is a 24-pin connector. Row C holds all analog signals, assuming that these pins are not used as digital inputs.

A supplemental contact row consisting of six connections is also mounted on the 2.54 mm grid. It is located next to the A-Terminal pins 14..24. Here the controller signals P4.3..P4.7 (A18..A23 or CAN-RX and CAN-TX) are available.

*Table 1* provides an overview of the pin assignments of the miniMODUL-connector.

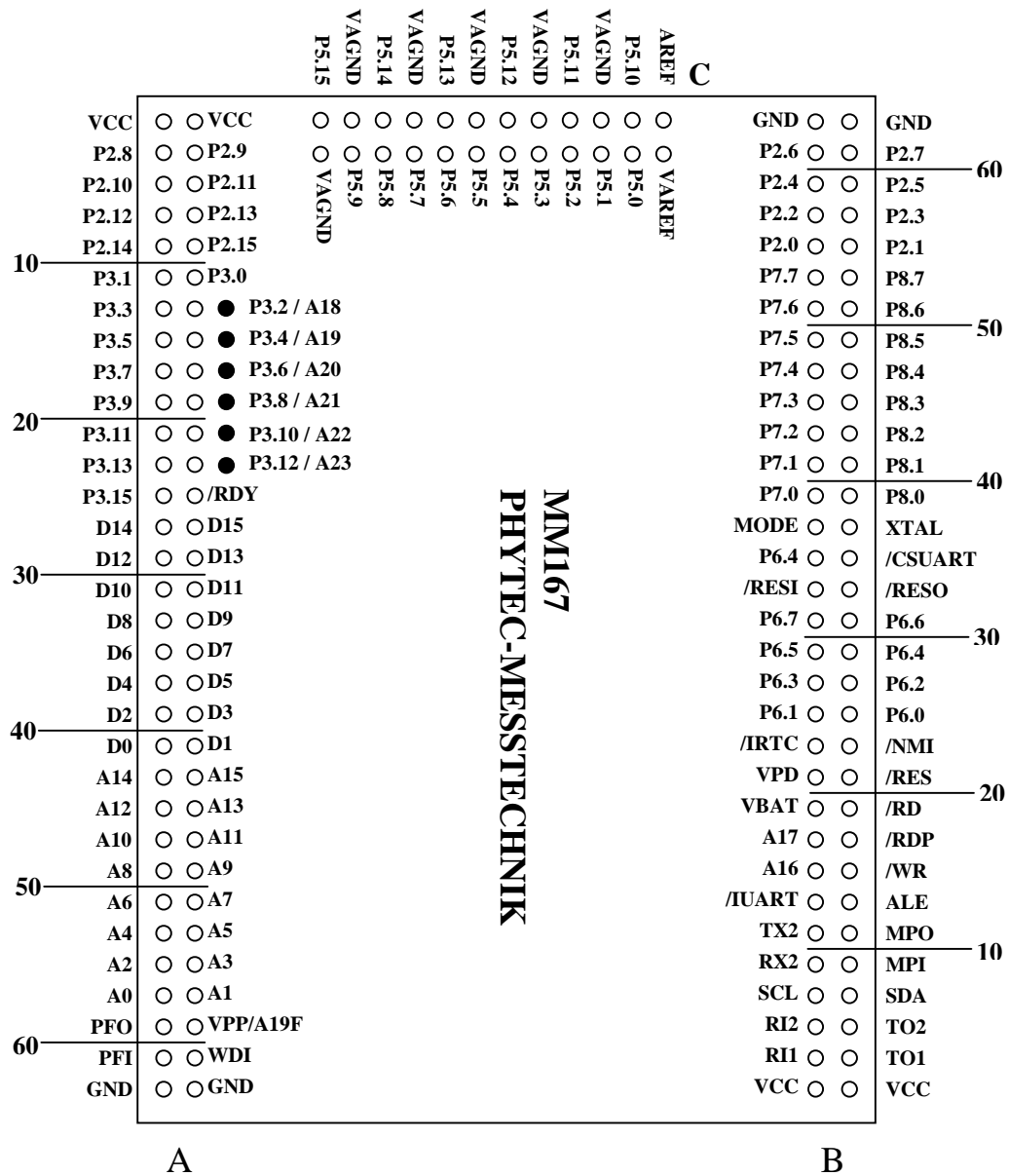


Figure 4: Pin-Layout

Interface	Name	Function
<b>Row A</b>	<b>left</b>	
A1, A2	Vcc	Supply voltage (+5 V +/-5 %, 500 mA)
A3..A10	P2.8..P2.15	C167 high-byte Port P2 (refer to C167 User's Manual)
A11, A12 A13, A14 A15, A16 A17, A18 A19, A20 A21, A22 A23, A24 A25	P3.1, P3.0 P3.3, P3.2 P3.5, P3.4 P3.7, P3.6 P3.9, P3.8 P3.11, P3.10 P3.13, P3.12 P3.15	C167 Port P3 (refer to C167 User's Manual)
A26	/RDY	C167 /Ready signal input (refer to C167 User's Manual)
A27..A42	D14, D15, D12, D13, D10, D11, ..., D0, D1	C167 Port P0 (refer to C167 User's Manual). This line should be connected over a 100 k $\Omega$ resistor at Vcc
A43..A58	A14, A15, A12, A13, ..., A0, A1	C167 Port P1 (refer to C167 User's Manual)
A59	PFO	MAX690 Power-Fail output (see section "UART, Real-Time Clock and Battery Buffering" of this manual)
A60	VPP / A19F	Programming voltage input only for 12 V Flash/(EP)ROM devices (U2..U5). This interface should normally remain unconnected.
A61	PFI	MAX690 Power-Fail input (see section "UART, Real-Time Clock and Battery Buffering" of this manual). If this input is not used, it must be connected to Vcc or GND.
A62	WDI	MAX690 Watchdog input (see section. "UART, Real-Time Clock and Battery Buffering" of this manual)
A63, A64	GND	Ground connection to the miniMODUL-167 (0-V.)
A65...A70	P4.2...P4.7	C167 Port P4.2 to P4.7 carry address lines A18..A23 or the on-chip CAN Interfaces (refer to C167 Derivatives User's Manual)

<b>Interface</b>	<b>Name</b>	<b>Function</b>
<b>Row B</b>	<b>left</b>	
B3	TO1	RS-232-level TxD output of the C167 internal asynchronous interface
B4	RI1	RS-232-level RxD input of the C167 internal asynchronous interface
B5	TO2	RS-232-level TxD output of the UART (refer to Philips SCC2691 data book)
B6	RI2	RS-232-level RxD input of the UART (refer to SCC2691 data book)
B7	SDA	RTC Data lines of the I <sup>2</sup> C Bus (refer to Philips PCF8583 data book)
B8	SCL	RTC Clock lines of the I <sup>2</sup> C bus (refer to PCF8583 data book)
B9	MPI	UART multipurpose input (refer to SCC2691 data book)
B10	RX2	UART RxD input (TTL levels of the RI2 inputs of the RS-232 interface)
B11	MPO	UART multipurpose input (refer to SCC2691 data book)
B12	TX2	UART TxD output (TTL levels of the TO2 output of the RS-232 interface)
B13	ALE	C167 ALE signal output (refer to C167 User's Manual)
B14	/IUART	UART /Interrupt output (open drain)
B15	/WR	C167 /WR signal output (refer to C167 User's Manual)
B16, B18	A16, A17	C167 Port P4.0, P4.1 (refer to C167 User's Manual)
B17	/RDP	C167 /RD signal output (refer to C167 User's Manual)
B19	/RD	/RD-signal-input for memory devices of the module (connected via J11 with /RDP)
B20	VBAT	Battery input for backup of RAM and RTC (see section 5.3, "Battery-Backup/Reset" of this manual).
B21	/RES	MAX690 /RESET output (open drain)

<b>Interface</b>	<b>Name</b>	<b>Function</b>
<b>Row B</b>	<b>right</b>	
B22	VPD	Output of the backup voltage (Vcc/VBAT) for buffering external components.
B23	/NMI	C167 /NMI output ( <i>refer to C167 User's Manual</i> ). This input must be connected with a Pull-up-resistor at Vcc.
B24	/IRTC	RTC /Interrupt output (open drain)
B25..B32	P6.0..P6.7	C167 Port P6 ( <i>refer to C167 User's Manual</i> ). P6.0..P6.4 is used for controller-internal /Csx-signals from the module ( <i>refer to the section 4, "Memory Models" in this manual</i> ).
B33	/RESO	C167 /RESOUT signal (Reset output) ( <i>refer to C167 User's Manual</i> ).
B34	/RESI	C167 /RESIN signal (Reset input) ( <i>refer to C167 User's Manual</i> ), connected to /RES by default
B35	/CSUART	UART /Chip Select-input (typically connected via J7 with P6.4 = /CS4 of the controller).
B36	P6.4	C167 /CS4 signal allowing compatibility with the PHYTEC miniMODUL-166 on this pin.
B37	XTAL	C167 XTAL1 signal output ( <i>refer to C167 User's Manual</i> ).
B38	MODE	Mode input of the decoder GAL (allowing the selection of a second memory model)
B39, B41,..B53	P8.0..P8.7	C167 Port P8 ( <i>refer to C167 User's Manual</i> )
B40, B42, ..B54	P7.0..P7.7	C167 Port P7 ( <i>refer to C167 User's Manual</i> )
B55..B62	P2.1, P2.0, P2.3, ..., P2.7, P2.6	C167 low byte Port P2 ( <i>refer to C167 User's Manual</i> )
B63, B64	GND	Ground connection of the miniMODUL-167 (0 V)

Row C	Top	
C1, C2	VAREF	C167 reference voltage input (+5 V, refer to C167 User's Manual)
C5, C9, C13, C17, C21,C24	VAGND	C167 analog ground input (0 V, refer to C167 User's Manual). Must be connected to GND-potential.
C4, C6, C8, C10, C12, C14, C16, C18, C20, C22 C3, C7, C11, C15, C19, C23	P5.0, P5.1, P5.2, P5.3, P5.4, P5.5, P5.6, P5.7, P5.8, P5.9 P5.10, P5.11, P5.12, P5.13, P5.14, P5.15	C167 Port P5 analog input (0 to 5 V/10-bit, refer to C167 User's Manual)

Table 1: Pinout of the miniMODUL-Connectors

## 2.1 ICE/Connect-167

When implementing the ICE/connect-167-interface (available from the vendor Hitex Development Tools, <http://www.hitex.com>), the following signals can be procured at the pin contact rows of the miniMODUL-167:

Interface	Pins
P0.0 - P0.15 = D0...15	A27..A42
P1.0 - P1.15 = A0...15	A43..A58
P4.0 - P4.7 = A16...A23	B16, B18, A65..A70
P6.0 - P6.4	B25..B29
ALE	B13
XTAL1	B37
/WR	B15
/BHE = P3.12	A24
/HLDA = P6.6	B31
+5 V = V <sub>cc</sub>	A1, A2, B1, B2
GND	A63, A64, B63, B64

Table 2: Pinout of the ICE/Connect-167

Several signals must be linked through the emulator. Unused signals can be disregarded.

<b>Interface</b>	<b>Explanation</b>	<b>Pin</b>
/RSTIN-P = /RESI	/RESIN-Controller	B34
/RSTIN-U = /RES	/RESIN-Environment	B21
/NMI-P = /NMI	/NMI-Controller	B23
/RD-P = /RDP	/RD-Controller	B17
/RD-U = /RD	/RD-Environment	B19
/RSTOUT-P = /RESO	/RESOUT-Controller	B33
/READY-P = /RDY	/READY-Controller	A26
/HOLD-P = P6.5	/HOLD-Controller	B30

Only the following signals are utilized on the miniMODUL-167 in conjunction with the ICE/connect-167:

<b>Interface</b>	<b>Pin</b>
/RSTIN-P, /RSTIN-U	B34 and B21, separated through J5
/RD-P, /RD-U	B17 and B19, separation through J11

We recommend using the Hitex adapter board to connect the PHYTEC miniMODUL-167 to the ICE/connect-167.



### **3 Jumpers**

To configure the module, the miniMODUL-167 has 12 solderable jumpers. In order to use the module immediately, the jumpers have been configured prior to delivery.

#### **J1**

J1 enables the selection of controller internal ROM/Flash according to the microcontroller mounted on the board. This jumper is always connected 2+3, as all standard PHYTEC modules are fitted with ROMless controllers.

J1 1+2 internal ROM/Flash-EPROM active

J1 2+3 internal ROM/Flash-EPROM inactive (standard)

#### **J2**

J2 produces a connection between Pin A23 (P3.13) and the /WR signal of the controller. With this, the pin compatibility of Pin A23 to the miniMODUL-166 can be made. In such a case, Port P3.13 may not be initialized as an output (which is also true of the miniMODUL-166). Normally this jumper is open, hence P3.13 of the C167 is fully functional.

J2 open Pin A23 = P3.13 (standard)

J2 closed Pin A23 = /WR (pin compatible to the MM-166)

#### **J3**

J3 enables selection of the installed RAM chips on U6/U7 or U8/U9. These jumpers depend on the memory size used and may not be changed.

J3 1+2 RAM Bank 1 (U6/U7) 1024kx8 Chips

J3 2+3 RAM Bank 1 (U6/U7) 4096kx8 Chips

#### **J4**

J4 enables selection of the installed Flash/(EP)ROM chips on U2/U3 and/or U4/U5, so that address line A19 of the controller or the Vpp-input of the miniMODUL-167 can be connected at Pin 1 of the memory device.

J4 1+2 Vpp for 12 V. Flash/(EP)ROM devices up to 2048k x 8

J4 2+3 A19 for Flash/(EP)ROM devices of 4096 x 8  
(1 MB bank)

#### **J5**

J5 separates the RESET signal of the miniMODUL-167 (/RES) from the RESET-input (/RESI) of the controller. Thus both signals are separated and available at pins B21 = /RES and B34 = /RESI and can be driven by in-circuit emulators (such as the ICE/connect-167 interface of Hitex Development Tool's T32 and AX166 emulators). This jumper is closed in normal operation.

#### **J6**

J6 controls the connection of the asynchronous serial interface (P3.11 = RxD) from the RS-232 driver on the miniMODUL-167. With this jumper, other driver select devices for interfacing can be used. The controller port can also function as regular I/O-port. Typically, this jumper is closed, hence configuring an RS-232 interface (pins B3 and B4 of the miniMODUL-167).

#### **J7**

J7 separates the connection between the /CS4 output of the controller and the chip select input (/CSUART) of the external UART (SCC2691) on the miniMODUL-167. With this, the UART can be addressed without further external address decoding from the controller. This jumper is closed upon delivery of the board. Should the user open this jumper, the /CS input of the UART (B35) must be connected to Vcc, or steered through another /CS signal.

## **J8**

J8 connects the interrupt outputs from the RTC and UART to port-pin P2.0 of the controller. With this, both devices with their open-drain outputs can trigger an active-low interrupt via Port P2.0 of the controller. With the jumper in the 1+2 position, the interrupt output of the external UART (SCC2691) is connected to Port P2.0 of the controller. With the jumper in the 2+3 position, the RTC can trigger an interrupt on Port P2.0. Both signals can also be combined with each other (J8: 1+2+3). In this case, the source of the interrupt via the status register of the RTC or the UART must be established in the controller by software.

## **J9 and J10**

J9 and J10 separate the RTC 12c bus from the port connections P2.1 and P2.2. The I<sup>2</sup>C bus of the RTC is already connected to ports P2.1 = SCL and P2.2 = SDA on the miniMODUL-167.

If just these port connections are required for other functions, port P2.1 can be separated from SCL on jumper J9. On J10, port P2.2 can likewise be separated from SDA of the RTC. In order to then use the RTC, an external connection must be made between another port and the signals SCL and SDA. The driver software must also be correspondingly adapted.

## **J11**

J11 separates the connections between B17 and B19 on the miniMODUL-167. These connections link the /RD signal of the controller (/RDP) with the /RD signal of the rest of the module. This connection can be opened to connect an emulator (ICE/connect-167) to the board. In order to operate the module without an emulator, both signals must be closed.

## J12

J12 selects the GAL-input for address decoding:

- |     |     |  |
|-----|-----|--|
| J12 | 1+2 | P6.0...3 = /CS0..3 for four memory banks (MODE = 1)  |
| J12 | 2+3 | A21 on GAL for decoding the 4 memory banks via addresses in GAL (/CS1...3 of the miniMODUL-167 are freely available) |

In the standard configuration of the miniMODUL-167, P6.3 (J12 1+2) is connected to GAL, which enables flexible address decoding with /CS signals of the controller for all four memory banks (*refer to section 4, "Memory Model MODE = 1"*). Additionally, with J12 = 2+3, the address line A21 can be connected to the GAL device, whereby address decoding to 4 MB is possible without controller-internal /CS signals (MODE = 0).

## 4 Memory Models

The C167 microcontroller has up to five Chip Select outputs (/CS0 to /CS4) which, can be initialized by software and assigned to various address areas during run time of the controller. This extremely flexible concept is expanded through a supplementary address decoder in the form of a GAL16V8-device on the miniMODUL-167. By configuring the MODE input of the miniMODUL-167, one of two memory models can be chosen. Setting MODE to 1, the /CS signals for the various memories are formed from the integral /CS signals and the A0 and /BHE signals. This means that the memory model is defined through the controller-internal mechanism by means of SFR ADDRSELx and BUSCONx. Setting MODE to 0, the memory model programmed in the GAL is chosen. Address decoding is done with address lines A18 to A21, without the controllers /CS signals, hence making these signals available as port connections for external digital extensions.

**Caution:**

Use of memory devices larger than 1024 x 8, requires the corresponding segment address-lines of the controller to be activated via configuration-resistance at P0H.3 and P0H.4 (D11, D12) during Reset (*refer to Table 3*).

The memory model of the standard GAL has the following functions:

MODE = 1:    /CS0    =    ROM-Bank 1,  
              /CS1    =    RAM-Bank 1,  
              /CS2    =    RAM-Bank 2,  
              /CS3    =    ROM-Bank 2.

In this mode the SFR ADDRSEL<sub>x</sub> and BUSCON<sub>x</sub> define the address areas for /CS0, /CS1, /CS2 and /CS3. As the memory model is defined by software this is a very flexible model. It is especially suitable for development using a debugger software development tools, as the program includes the software for configuring the memory model.

**Caution:**

Using this mode, please note:

Following a reset, only the /CS0 connection is available for accessing the entire address area of the controller (in MODE = 1, ROM-Bank-1 = U2/3). /CS0 is always active in those areas in which no other /CS<sub>x</sub>-signals are active. To access additional /CS<sub>x</sub>-signals of the C167, the corresponding ADDRSEL<sub>x</sub> register must be configured for the desired address area. Only after doing this, the BUSCON<sub>x</sub>-register can be configured in order to activate the corresponding /CS<sub>x</sub>-signal.

Note that no /CS<sub>x</sub>-signals must overlap and that the area of the program code within /CS0 cannot be superceded by another /CS<sub>x</sub>-signal.

MODE = 0:    /CS0 + /A18+ /A19 = ROM-Bank 1, (256 kByte)  
              /CS0 + A18 + /A19 = RAM-Bank 1, (256 kByte)  
              /CS0 + /A18 + A19 = RAM-Bank 2, (256 kByte)  
              /CS0 + A18 + A19 = ROM-Bank 2, (256 kByte)

This alternate model (MODE = 0) is especially suitable for final operation with the finished software in the Flash memory. Since the internal address-decoder of the controller is not used, the only delay time occurring is that of the GAL between the address signals of the controller and the activation of the Chip Select signals of the memory chips. The /CS signals of the C167 (/CS0.../CS4) can be used for external connection to the miniMODUL-167.

Two examples for configuring the memory of the miniMODUL-167 are provided below.

a) Configuration: MODE = 1 (controller-internal /CS signals)

ADDRSEL1 = 0406h: /CS1 4:000-7:FFFFh (256 kByte RAM-1)  
ADDRSEL2 = 0806h: /CS2 8:000-B:FFFFh (256 kByte RAM-2)  
ADDRSEL3 = 0C06h: /CS3 C:000-F:FFFFh (256 kByte ROM-2)  
ADDRSEL4 = 1000h: /CS4 10:000-10:0FFFh (4 kByte UART)

BUSCON0 = 04AEh Bus active for /CS0 (ROM-Bank-1)  
BUSCON1 = 04AEh Bus active for /CS1 (RAM-Bank-1)  
BUSCON2 = 04AEh Bus active for /CS2 (RAM-Bank-2)  
BUSCON3 = 04AEh Bus active for /CS3 (ROM-Bank-2)  
BUSCON4 = 060Dh Bus active for /CS4 (UART)

b) Configuration: MODE = 0 (external /CS signals from GAL)

BUSCON0 = 04AEh, BUSCON1..4 = 0000h CS1.../CS4 not active

Segment addresses A16..A19 must be activated (POH3 = d11 = 0)!

These memory models are illustrated in the following diagram:

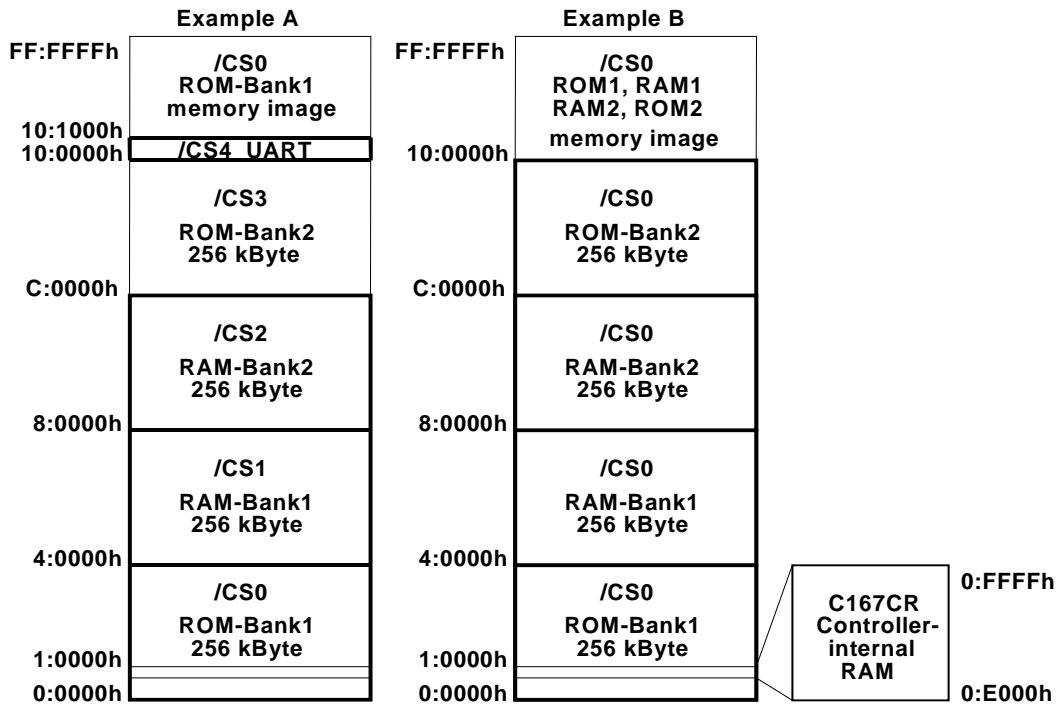


Figure 5: Memory Models

## 4.1 Bus-Timing

For connecting additional peripheral hardware the boards recommended values for the BUSCONx registers are:

BUSCONx: 04AEh = 1 Wait-States, RW-delay, no tri-state short ALE, 16-bit demultiplexed, address-/CSx, active (for memory devices running up to 70 ns on the miniMODUL-167)

This configuration uses one Wait-State and the RW-delay. When using one Wait-State ( $T_c = 50$  ns) and the RW-delay, all memories must respond within an access time of 70 ns at a bus cycle time of 150 ns.

In order to be able to use the controller without Wait-States, decoding must be executed only with the external GAL(16V8-10). In this case, the controller's internal /CS signals must remain unused and memories with a maximum of 55 ns access time are required on the module.

**Note:**

At the moment, the miniMODUL-167 is equipped with a 70 ns Flash memory and a 70 ns RAM. This configuration only allows operation with a minimum of one wait state and RW-delay.

Important signal times in 16-bit bus non-multiplexed mode at 20 MHz clock frequency ( $F_{osc}$ ) are:

- $T_c = 50 \text{ ns} \times \text{Wait-states control (MCTC in BUSCON)}$
- $T_f = 50 \text{ ns} \times \text{Tri-state control (MTTC in BUSCON)}$
- Addresses stable for valid data max.    max 70 ns +  $T_c$     SR<sup>1</sup>
- /RD low for data valid max                max 55 ns +  $T_c$     SR<sup>1</sup>
- /RD low for data valid (/RW-delay)    max 30 ns +  $T_c$     SR<sup>1</sup>
- /RD high for databus high-Z            max 15 ns +  $T_f$     SR<sup>1</sup>
- /RD high for data high-Z (RW-delay) max 35 ns +  $T_f$     SR<sup>1</sup>
- /CS for data valid                            min 55 ns +  $T_c$     SR<sup>1</sup>
- /RD and /WR low                            min 65 ns +  $T_c$     CC<sup>2</sup>
- /RD and /WR low (RW-delay)            min 40 ns +  $T_c$     CC<sup>2</sup>
- /WR-low for data valid                    min 25 ns +  $T_c$     CC<sup>2</sup>
- /WR high for data invalid                min 15 ns +  $T_f$     CC<sup>2</sup>

<sup>1</sup> SR = System request: requests must be kept from switching the C167

<sup>2</sup>: CC = Controller characteristic: the controller guarantees these times for turn-off



## 5 Usage Hints for the miniMODUL-167

### 5.1 External Digital Interface

Any 167-derivative controller (C167CR, C167CS, etc.) can be fitted on the miniMODUL-167. Please note that when using the on-chip CAN interface, only 20 external address lines (A0..A19), and hence 1 MB of associated address space per /CSx signal, is available. By using all /CS connections, a maximum of 5 MB can be addressed. If address lines A18..A23 are used, a port 0 configuration resistor (e.g. 4k $\Omega$  to GND) at P0H3 is necessary.

Address and data buses extend from the controller to the pin headers at the edges of the board without any buffer. When connecting external chips to the data/address bus as well as to the control lines (/RD, /WR), the user should provide external buffers (such as the 74AHCT245) to these signals between the module and the peripheral devices.

The data bus D0..15 (Port 0) should be attached to the Vcc through a 100k pull-up-resistor. You should provide for the possibility of attaching pull-down resistors directly to Port 0 (Pin 0..15) to set the processor configuration. This makes it possible to start the C167 in different configurations, as these pins are read during reset (*refer to the C167 User's Manual*). Such a resistor is already provided on the miniMODUL-167 at Port POL.6, allowing the non-multiplexed mode for the data/address bus to be set. The user must provide an additional resistor via a jumper at Port POL.4 to enable the C167 to start by means of the internal Bootstrap Loader. This allows the chip-internal Bootstrap Loader to be started each time by closing a jumper. This is necessary, for instance, when programming a Flash memory from software updates or when downloading an application program via the FlashTools download utilities. A Monitor program can also be started via the Bootstrap Loader.

## P0 Configuration Functions (\* = module standard configuration)

Port Pin	Function, if R = 4.7k to GND	Read at:
P0L.0	Emulation Mode	Hardware-Reset
P0L.1	Adapt Mode (ONCE mode)	Hardware-Reset
P0L.4	Bootstrap Loader Mode	Hardware-Reset
P0L.6	* - Bus Mode (Non-Multiplexed)	HW-/SW- Reset
P0L.7	Data-bus width (8-bit Data bus)	HW-/SW- Reset
P0H.1 P0H.2	Number of /CSx signals at Port P6 * - P0H2, P0H1 = 1, 1 = 5 (/CS0../CS4) P0H2, P0H1 = 1, 0 = 0 (no /CS) P0H2, P0H1 = 1, 1 = 2 (/CS0, /CS1) P0H2, P0H1 = 1, 0 = 3 (/CS0../CS2)	HW-/SW- Reset
P0H.3 P0H.4	Number of segment address lines on Port P4 * - P0H4, P0H3 = 1, 1 = 2 (A16, A17) P0H4, P0H3 = 1, 0 = 8 (A16..A23) P0H4, P0H3 = 0, 1 = 0 (no /CS) P0H4, P0H3 = 0, 0 = 4 (A16..A19)	HW-/SW- Reset
P0H.5 P0H.6 P0H.7	Clock mode / PLL factor (not available on all C167 controllers)	HW-/SW- Reset

Table 3: Configuration of the Controller via P0

For additional information on P0 configuration functions, refer to the C167 User's Manual.

The NMI-input should have a pull-up resistor (10 K) to Vcc. The NMI can thus be tripped with a falling edge (e.g. with a push button to ground) which is useful in software development via a Monitor program.

Do not connect the Vpp-Pin to a 12 V power source given the standard configuration of the miniMODUL-167, which is fitted with 5 V Flash memory device (either type 29F010 or 29F040 from Advanced Micro Devices).

If a larger memory device (>1024 x 8) is fitted onto the module, or if the memory model MODE = 0, the segment addresses A18..A19(A23) must be freely switched at Port P0H.3 (P0H.4).

## **5.2 Memory Access Times and Memory Configuration**

The standard miniMODUL-167 operates in a 16-bit non-multiplexed mode and uses the signals A0 and /BHE for bus access (produced by the chip) to the low- and high-bytes in the memory. A target memory access is also possible by byte.

In memory sockets U2/U3 and U4/U5, Flash memories of 256k x 8 to 4096k x 8 can be fitted in the PLCC32 housing. Pin-compatible (EP)ROM devices (1024k x 8 to 2048k x 8) can also be inserted into these same sockets. U2/U3 represents the first ROM bank. U4 and U5 comprise the second ROM bank. U6 and U7 are designated as the first RAM bank and can be populated with 1024k x 8 or 4096k x 8 SRAM in an SO32 housing. This RAM bank can be buffered via an external battery. U8/U9 form the second RAM bank and can be populated with memory chips similar to those used in U6/U7.

Please note the maximum controller speed cannot be attained with the chips currently installed on the miniMODUL-167. In view of the timing of the controller and the 70 ns access capability of the Flash memory (and RAM), we recommend that the user program one wait state and one RW-delay in the corresponding BUSCONx registers. For control of the /CS signals to the memories, the integral Chip Select signals (P6.0..3) are used. These signals produce a delay of about 20 ns on the address signals. If the user desires to run exceptionally quick routines, then these routines should be run out of a RAM bank on the module (one wait state). An alternate is to do the address decoding (Chip Select signals) exclusively via the GAL (max. 10 ns) and to install faster memory chips (Flash and RAM with max. 55 ns) on the module.

In the standard memory configuration (MODE =1) of the miniMODUL-167, the first Flash memory bank is addressed with the /CS0 signal of the controller; /CS1 selects the module's first RAM bank and the second RAM bank is enabled via the /CS2 of the controller. /CS3 accesses the second Flash-EPROM-bank. /CS4 controls the UART (SCC2691).

In MODE = 0 on the miniMODUL-167, memories are only selected through the address lines of the controller (A18..A23) and through the /CS0 signal (*refer to section 3, "Memory Models" of this manual*).

**Caution:**

Use of memory devices larger than 1024 x 8, requires the corresponding segment address-lines of the controller to be activated via configuration-resistance at P0H.3 and P0H.4 (D11, D12) during Reset.

### 5.3 UART, Real-Time Clock and Battery Buffering

The external UART (additional serial interface of the miniMODUL-167) is selected via the controllers chip select signal /CS4 on port P6.4 (*refer to section 3*). The chip is only fully addressable in 8-bit mode, configuration: BUSCON4 = 060Dh (8-bit demultiplexed, RW-delay, Tristate-Wait, long ALE, two Wait-states). A driver for the operation of the chip is supplied on the enclosed Spectrum CD included with the miniMODUL-167. The interrupt-output (open-drain) of the UART (/IUART = PIN B14) can be set via jumper J8 (1+2) onto Port P2.0 of the controller.

The RTC is addressable via the port bits P2.1 = SCL and P2.2 = SDA, using an I<sup>2</sup>C-bus protocol. The interrupt output of the RTC can, as with the UART-interrupt, be set with Jumper J8 on Port P2.0. Here J8 should be bridged between 2 and 3. It is possible to put both interrupt-outputs (UART and RTC) on Port 2.0 of the C167, since both have an open-drain output and the interrupt-source can be determined via the corresponding status register of the chips. All signals are available via the pins to the edge of the board.

A constant voltage source of 3-4 V. must be connected to the VBAT input (Pin B20) in order to maintain and receive data from the Real-Time Clock (RTC) independently from the Vcc, as well as to back-up data in the first RAM bank. The power consumption requirement of the miniMODUL-167 is less than 200 µA (typically 5 µA.) at a temperature of 20 °C.

The miniMODUL-167 is equipped with a POWER-FAIL-mechanism, hence allowing early detection of interruptions in the power supply. The input voltage at PFI (A61) is compared with an internal 1.3 V reference voltage and - in the event of a reduction of input voltage - switches the PFO-output against the GND. Should the battery buffer or Power-Fail-mechanism not be utilized, the VBAT-input (or the PFI-input) must be connected to the GND.

If the WDI-input is connected, then the pin at WDI must toggle at least once a second. Otherwise, the Watchdog of the MAX690 triggers a RESET of the miniMODUL-167. Should the Watchdog not be engaged, then the WDI-input must remain unconnected.



## 6 Technical Specifications

The physical dimensions of the miniMODUL-167 are represented in *Figure 6*. The module's profile about 10 mm thick, with a max. height of the components of 5 mm on the soldering-side as well as on the component-side. The board itself is approx. 1.5 mm thick.

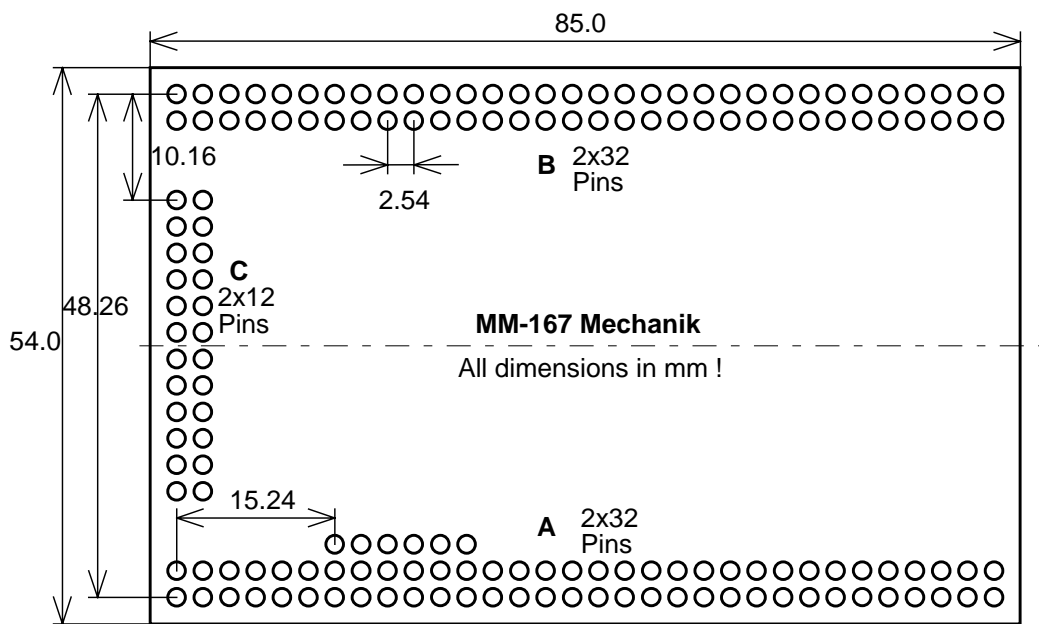


Figure 6: Physical Dimensions

Additional specifications:

- Voltage: 5 V +/- 5 %
- Power Requirements: max. 500 mA. (typ. 160 mA)  
(at Ta = 20°C, Fosc = 20 MHz,  
Vcc = 5 V)
- Storage Temperature: -40 to +90 °C
- Operating Temperature: 0 to +70 °C
- Humidity (rel.): 0 % to 95 % non-condensing
- Dimensions.: 85 x 54 x 15 mm. (l x b x h) +/- 1 mm.  
IC height above/  
below the board: max 5 mm.

**Note:**

This data specifically refers to the standard configuration of the miniMODUL-167. Its typical power requirement is lower than 160 mA (*refer to table below*).

Standard Board MM-310 with standard GAL device 16V8H-15

RUN (Monitor runs out of RAM)	155 mA
RESET	125 mA
IDLE	95 mA
POWERDOWN	55 mA

Board with zero-power GAL device 16V8Z-15

RUN (Monitor runs out of RAM)	120 mA
RESET	90 mA
IDLE	60 mA
POWERDOWN (all /CS = high)	10 – 15 mA depending on the RS-232 driver
POWERDOWN (without RS232)	1 – 2 mA

**Note:**

Take precautions to heed ESD-recommendations when handling the minMODUL's CMOS components.

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**How would you improve this manual?**

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**Did you find any mistakes in this manual?** \_\_\_\_\_ page

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