

phyCORE-SC520

Hardware Manual

Edition June 2002

In this manual are descriptions for copyrighted products that are not explicitly indicated as such. The absence of the trademark (™) and copyright (©) symbols does not imply that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual.

The information in this document has been carefully checked and is believed to be entirely reliable. However, PHYTEC Meßtechnik GmbH assumes no responsibility for any inaccuracies. PHYTEC Meßtechnik GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product. PHYTEC Meßtechnik GmbH reserves the right to alter the information contained herein without prior notification and accepts no responsibility for any damages which might result.

Additionally, PHYTEC Meßtechnik GmbH offers no guarantee nor accepts any liability for damages arising from the improper usage or improper installation of the hardware or software. PHYTEC Meßtechnik GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

© Copyright 2002 PHYTEC Meßtechnik GmbH, D-55129 Mainz.

Rights - including those of translation, reprint, broadcast, photomechanical or similar reproduction and storage or processing in computer systems, in whole or in part - are reserved. No reproduction may occur without the express written consent from PHYTEC Meßtechnik GmbH.

	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 info@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

2nd Edition June 2002

Preface	1
1 Introduction	3
1.1 Block Diagram.....	7
1.2 View of the phyCORE-SC520.....	8
2 Pin Description	9
2.1 Supply Voltage	20
2.2 AMDebug Interface.....	22
2.3 Serial Interfaces	23
2.4 Infrared Interface	25
2.5 Parallel Interface.....	26
2.6 Floppy Interface.....	27
2.7 IDE Interface	28
2.8 Keyboard and Mouse Interfaces	28
2.9 Ethernet Connector	29
2.10 SSI Interface	29
2.11 ISA Bus.....	30
2.12 PCI Bus.....	32
3 System Configuration	33
3.1 Memory Mapping	33
3.2 Interrupts.....	34
3.3 DMA Channels	36
3.4 Chip Select Signals.....	37
3.5 Programmable Address Region Register.....	38
3.6 SIO Initialization	39
4 System-BIOS	41
4.1 Various Boot Modes.....	41
4.2 CMOS Setup.....	42
4.3 Flash Disk	43
4.4 Manufacturing Mode	44
4.4.1 Access to Drives Configured in the BIOS (i.e. Flash Disk)	44
4.4.2 Direct Access to the Flash Device.....	47
5 Technical Specifications	53

6	Hints for Handling the phyCORE-SC520.....	55
7	Connection Examples for External Periphery	57
7.1	Connecting a Serial Device to the SSI Bus	57
7.1.1	3-Wire Connection	57
7.1.2	4-Wire Connection	57
7.2	Connecting a Hard-Drive	58
7.3	Connecting a Floppy-Drive	58
7.4	Connecting a Keyboard	59
7.5	Connecting a Mouse	59
7.6	Connecting the Serial Interfaces.....	59
7.7	Connecting the Parallel Interface	60
7.8	Connecting an Infrared Transmit/Receive Unit	61
7.8.1	Connection at COM4 Pins.....	61
7.8.2	Connecting at SIO GP Pins	61
7.9	Ethernet Connection	62
7.10	Connecting the Boot Jumper	62
	Index.....	63

Index of Figures

Figure 1: Block Diagram phyCORE-SC520 7

Figure 2: View of the phyCORE-SC520..... 8

Figure 3: Pinout of the phyCORE-Connector
 (Top View, with Cross Section Insert) 11

Figure 4: Pinout of the AMDebug-Connector X2..... 22

Figure 5: System BIOS Setup-Utility Window 42

Figure 6: Physical Dimensions..... 53

Figure 7: SSI Bus, 3-Wire Connection (Example)..... 57

Figure 8: SSI Bus, 4-Wire Connection (Example)..... 57

Figure 9: Connecting a Hard-Drive (Example)..... 58

Figure 10: Connecting a Floppy-Drive (Example)..... 58

Figure 11: Connecting a Keyboard (Example)..... 59

Figure 12: Connecting a Mouse (Example) 59

Figure 13: Connecting the Serial Interfaces COMx (Example)..... 59

Figure 14: Connecting the Parallel Interface (Example)..... 60

Figure 15: Connecting an Infrared Module (Example with COM4 Pins).... 61

Figure 16: Connecting an Infrared Module (Example with SIO GP Pins) .. 61

Figure 17: Ethernet Connection (Example) 62

Figure 18: Connecting the Boot Jumper (Example)..... 62

Index of Tables

Table 1: Pinout of the phyCORE-Connector X1	19
Table 2: Supply Voltage Connections	20
Table 3: Current Draw	21
Table 4: Pinout of the AMDebug-Connector X2	22
Table 5: Pinout of the Serial Interface COM1 (V24)	23
Table 6: Pinout of the Serial Interface COM2 (V24)	24
Table 7: Pinout of the Serial Interface COM3 (5 V TTL).....	24
Table 8: Pinout of the Serial Interface COM4 (5 V TTL).....	24
Table 9: Pinout IR Interface on COM4 Pins	25
Table 10: Pinout IR Interface on I/O Pins	25
Table 11: Pinout of the Parallel Interface	26
Table 12: Pinout of the Floppy Interface	27
Table 13: IDE-Specific Signals	28
Table 14: Keyboard Interface	28
Table 15: Mouse Interface	28
Table 16: Ethernet Connector	29
Table 17: Pinout of the SSI Interface	29
Table 18: PCI Bus.....	32
Table 19: Memory Mapping	33
Table 20: Interrupt Configuration.....	34
Table 21: Interrupts on the Molex Connector X1.....	35
Table 22: DMA Connections.....	36
Table 23: Chip Select Configuration	37
Table 24: PAR Register Configuration	38
Table 25: Super I/O Interrupt and DMA Configuration.....	39

Preface

This phyCORE-SC520 Hardware Manual describes the board's design and functions. Precise specifications for the "Elan SC520" controller series can be found in the enclosed microcontroller Data Sheet/User's Manual from AMD as well as the documentation for peripheral components: "FDC37B787, Enhanced Super I/O Controller with ACPI Support, Real-Time Clock and Consumer IR" from SMSC and "RTL8139C, Single Chip Fast Ethernet Controller with Power Management" from Realtek. If software is included also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformance of the PHYTEC phyCORE-SC520



PHYTEC Single Board Computers (henceforth "products") are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, are subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-SC520 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations.

PHYTEC supports all common 8- and 16-bit as well as specific 32-bit controllers in two ways:

- (1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
- (2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-SC520 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments, the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

We at PHYTEC consider it our responsibility, as a reliable partner and ISO 9001 certified supplier, to enable the integration of our insert ready microcontroller modules into your OEM production. This is an important condition for the success of our product.

The phyCORE-SC520 is a subminiature (60 x 53 mm) insert-ready Single Board Computer populated with the Elan SC520 microcontroller from AMD.

Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a “big chip” into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User’s Manual or Data Sheet. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-SC520.

The phyCORE-SC520 offers the following features:

- subminiature Single Board Computer (60 x 53 mm) achieved through modern SMD technology
- 586-compatible CPU with a Floating Point Unit and 16 kByte write back cache
- 133 MHz clock frequency (core)
- Low Voltage Operation ($VCC_{core} = 2.5 \text{ V}$)
- Integrated PCI controller for 33 MHz 32-bit PCI Bus (Version 2.2), supports up to 5 external PCI masters
- SDRAM controller for up to 256 MB, 66 MHz clock
- Expanded JTAG port (AMDebug) with the possibility of debugging and executing individual steps during operation.
- General Purpose (GP) Bus with programmable timings
- ROM / FLASH controller for 8-, 16-, 32-bit data bus width
- PC/AT compatible periphery units: 22 prioritizable interrupt channels (15 external inputs), expandable DMA controller, 2 modem capable UARTs.
- Real-Time Clock with 114 Byte CMOS-RAM with battery buffering
- Additional integrated periphery: 3 cascaded and freely programmable 16-bit timers, watchdog and software timers, Synchronous Serial Interface
- 32 programmable I/O-Pins
- Support of Windows CE, pSOS, QNX, RTX, and VxWorks operating systems
- Industry standard BIOS support
- Improved interference protection via multilayer technology as well as reduced radiation interference due to improved ground connections.
- All ports as well as data and address lines extend to two 160-pole high density (0.635 mm) Molex connectors located on the underside of the Development Board
- Can be inserted into target circuitry like a "big chip"

- On-board Flash programming
- No separate programming voltage for use with 3.3 V Flash devices
- 16 MB – 64 MB DRAM on-board
- 1 MB (up to 4 MB) Flash on-board
- 128 Byte to 2 kByte serial EEPROM
- Voltage Supervisor Chip for Reset Logic
- Battery monitoring
- 8 Chip Select signals extending to Molex connectors
- 2 DMA channels extending to Molex connectors
- 19 I/Os extending to Molex connectors
- 9 IRQ inputs extending to Molex connectors
- PC/AT compatible **Programmable Interval Timer (PIT)** for system loud speaker
- Supply voltages: 5 V, 3.3 V, 2.5 V

- Populated with **Super Input Output (SIO)** device FDC37B787
 - ISA Plug and Play compatible register chain
 - Multi faceted power management
 - 8042 keyboard controller
 - Real-Time Clock
 - 2.88 MB **Floppy Disc Controller**
 - 2 modem capable UARTs
 - Infrared interface supporting the following formats: IrDA 1.0, Consumer IR< HP-SIR, ASK-IR
 - Parallel port

- Populated with Ethernet controller RTL8139
 - 10 MB/s and 100 MB/s operation
 - PCI version 2.2 compatible
 - Supports ACPI and PCI power management
 - PC99 standard compatible
 - Supports Wake-on-LAN and remote wake-up (Magic Packet, LinkChg and Microsoft wake-up frame)
 - External serial EEPROM for storing the configuration and identification data

1.1 Block Diagram

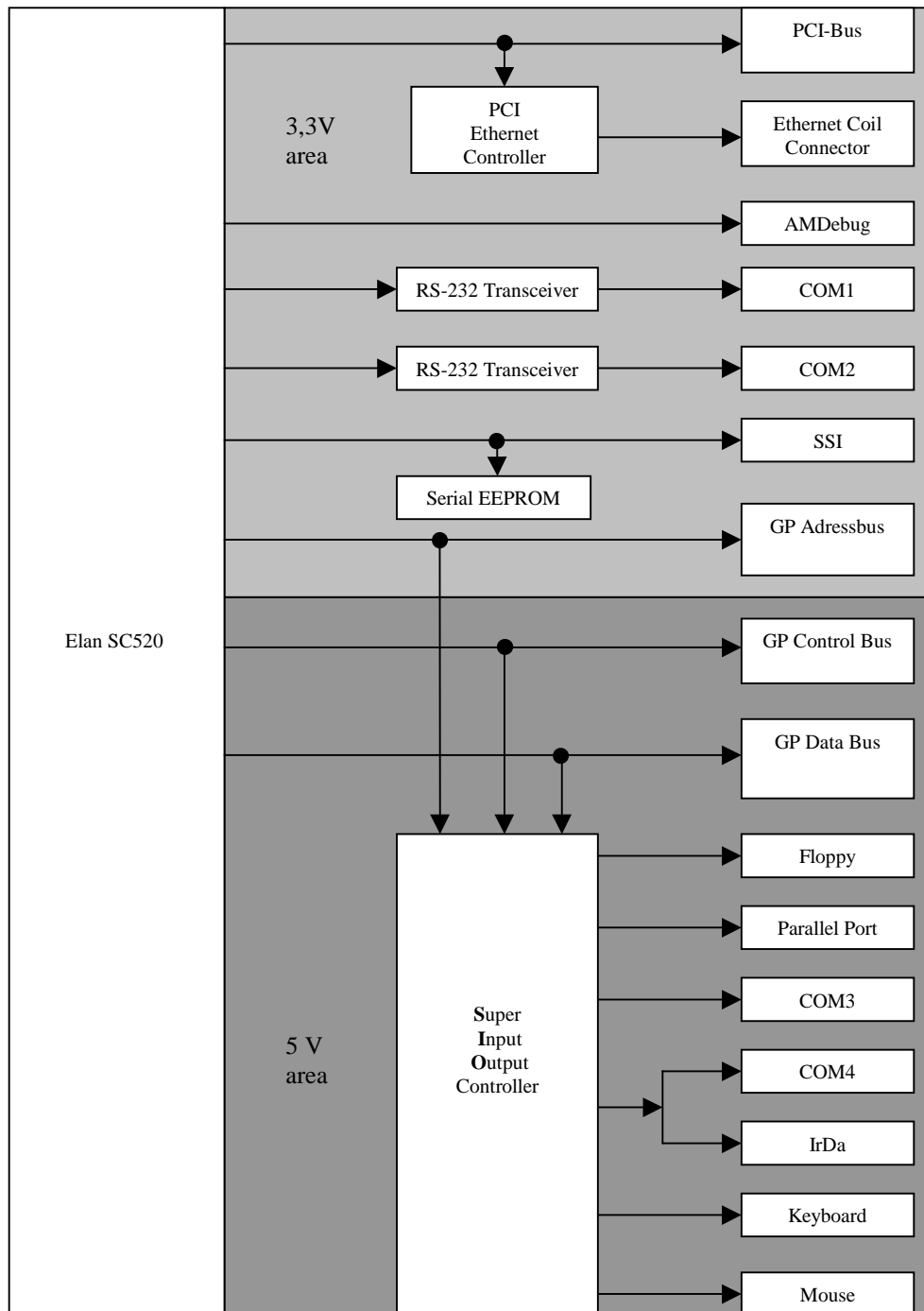


Figure 1: Block Diagram phyCORE-SC520

1.2 View of the phyCORE-SC520

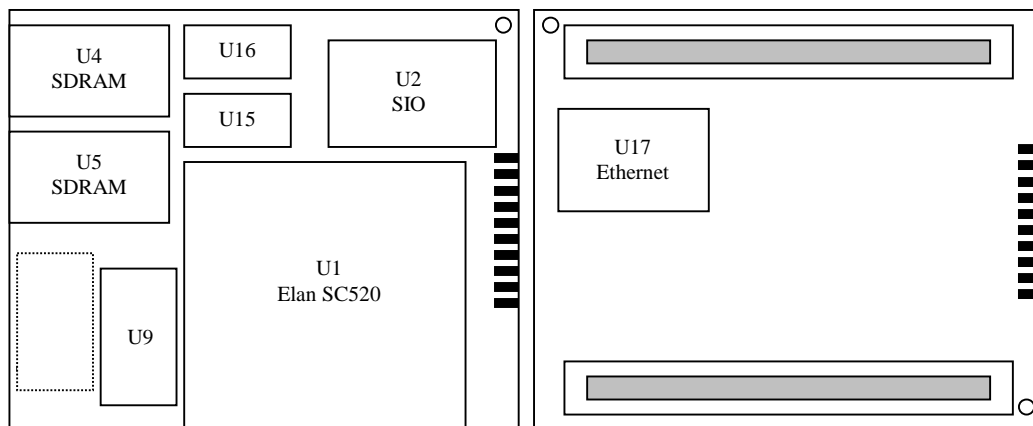


Figure 2: View of the phyCORE-SC520

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 3* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-SC520 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE-module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 3*).

The numbered matrix can be aligned with the phyCORE-SC520 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-SC520 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

The following figure (*Figure 3*) illustrates the numbered matrix system. It shows a phyCORE-SC520 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board.

In order to facilitate understanding of the pin assignment scheme, the diagram presents a crossview of the phyCORE module showing these phyCORE-connectors mounted on the underside of the module's PCB.

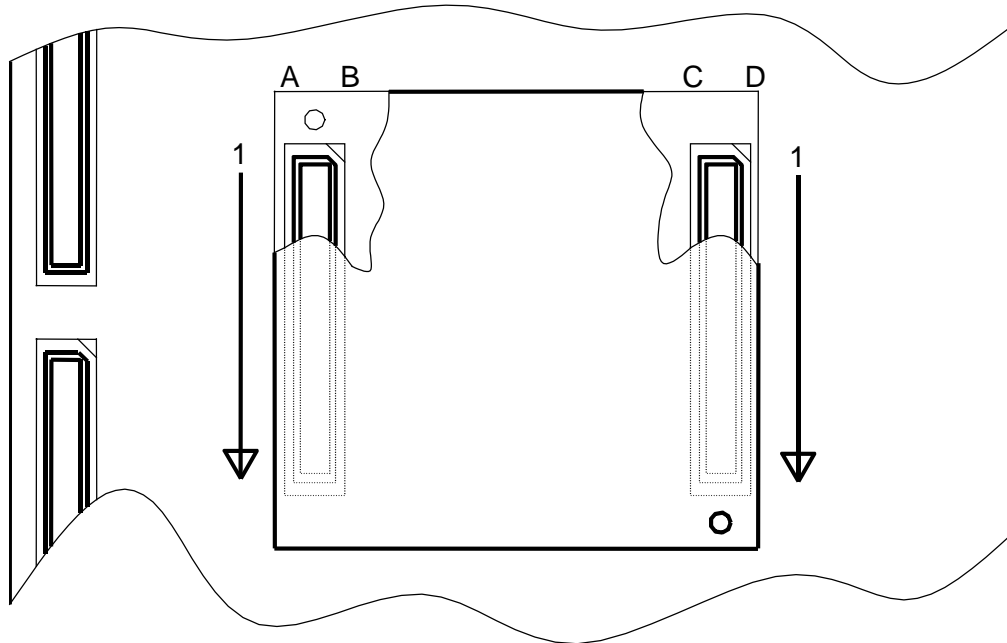


Figure 3: Pinout of the phyCORE-Connector (Top View, with Cross Section Insert)

Many of the controller port pins accessible at the connectors along the edges of the board have been assigned alternate functions that can be activated via software.

Pin #	Signal	I/O	Description
Row X1A			
1A	CLKIN	I	Optional external clock generator
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground
3A	GPIRQ1	I	GP Bus Interrupt Request 1 or PIO 22, Interrupt input 1 or programmable in-/output 22
4A	GPIRQ5	I	GP Bus Interrupt Request 5 or PIO 18, Interrupt input 5 or programmable in-/output 18
5A	/GPCS1	O	Chip Select 1, can be used for external Flash
6A	GPALÉ	O	GP Bus Address Latch Enable, displays valid addresses on the address bus
8A	/GPIOWR	O	GP Bus I/O Write, shows write access to I/O device
9A	GPA1	O	General-Purpose Address Bus, Address bus for memory, I/O and external Flash devices, GP address line 1
10A	GPA2	O	GP address line 2
11A	GPA4	O	GP address line 4
13A	GPA7	O	GP address line 7
14A	GPA9	O	GP address line 9
15A	GPA10	O	GP address line 10
16A	GPA12	O	GP address line 12
18A	GPA15	O	GP address line 15
19A	GPD1	I/O	General Purpose Data Bus, Data transfer during memory or I/O read or write accesses, GP data line 1
20A	GPD2	I/O	GP data line 2
21A	GPD4	I/O	GP data line 4
23A	GPD7	I/O	GP data line 7
24A	GPA17	O	GP address line 17
25A	GPA18	O	GP address line 18
26A	GPA20	O	GP address line 20
28A	GPA23	O	GP address line 23
29A	GPD9	I/O	GP data line 9
30A	GPD10	I/O	GP data line 10
31A	GPD12	I/O	GP data line 12
33A	GPD15	I/O	GP data line 15
34A	GPA25	O	GP address line 25
35A	GPRDY	I	GP Bus Ready, with a „Low“ GP enters Bus Wait States
36A	/GPMEMRD	O	GP Bus Memory Read, write access to selected memory components
38A	GPTC	O	GP Bus Terminal Count, DMA Transfer counter is zero, last transfer cycle
39A	/GPIOCS16	I	GP Bus I/O Chip Select 16, I/O component awaits 16-bit access
40A	/GPDBUFOE	O	GP Bus Data Buffer Output Enable, shows access to GP Bus

Pin #	Signal	I/O	Description
Row X1A			
41A		-	NC, should remain disconnected
43A	PCI-AD1	I/O	PCI Address Data Bus, time multiplexed address and data bus, PCI address-/dataline 1
44A	PCI-AD3	I/O	PCI address/data line 3
45A	PCI-AD4	I/O	PCI address/data line 4
46A	PCI-AD6	I/O	PCI address/data line 6
48A	PCI-AD9	I/O	PCI address/data line 9
49A	PCI-AD11	I/O	PCI address/data line 11
50A	PCI-AD12	I/O	PCI address/data line 12
51A	PCI-AD14	I/O	PCI address/data line 14
53A	PCI-AD17	I/O	PCI address/data line 17
54A	PCI-AD19	I/O	PCI address/data line 19
55A	PCI-AD20	I/O	PCI address/data line 20
56A	PCI-AD22	I/O	PCI address/data line 22
58A	PCI-AD25	I/O	PCI address/data line 25
59A	PCI-AD27	I/O	PCI address/data line 27
60A	PCI-AD28	I/O	PCI address/data line 28
61A	PCI-AD30	I/O	PCI address/data line 30
63A	/PCI-FRAME	I/O	Frame, Initiator shows start and duration of the transaction on the bus
64A	/PCI-CBE1	I/O	Command or Byte-Enable Bus 1
65A	/PCI-CBE2	I/O	Command or Byte-Enable Bus 2
66A	PCI-PAR	I/O	Parity, is set by the initiator
68A	/PCI-DEVSEL	I/O	Device Select, set by target, if it has recognized the address
69A	/PCI-REQ1	I	Bus Request, Master 1 wants bus access
70A	/PCI-GNT1	O	Bus Grant 1, bus access for Master 1 granted
71A	/PCI-REQ3	I	Bus Request, Master 3 wants bus access
73A	/PCI-GNT4	O	Bus Grant 4, bus access for Master 4 granted
74A	/PCI-INTA	I	Interrupt Request, PCI Interrupt A
75A	/PCI-INTC	I	Interrupt Request, PCI Interrupt C
76A	PCI-CLK0	O	PCI Clock line 0
78A	PCI-CLK2	O	PCI Clock line 2
79A	PCI-CLK3	O	PCI Clock line3
80A	/PCI-PERR	B	Parity Error, a parity error has occurred on the bus

Pin #	Signal	I/O	Description
Row X1B			
1B	OSC14M	O	14.318 MHz clock
2B	GPIRQ0	I	GP Bus Interrupt Request 0 or PIO 23, Interrupt input 0 or programmable in-/output 23
3B	GPIRQ2	I	GP Bus Interrupt Request 2 or PIO 21, Interrupt input 2 or programmable in-/output 21
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND	-	Ground
5B	/GPCS2	O	Chip Select, can be used for external Flash
6B	/GPCS4	O	GP Chip Select, can address memory or I/O devices or be configured as timer input 1
7B	/GPIORD	O	GP Bus I/O Read, shows read access on I/O device
8B	GPA0	O	GP address line 0
10B	GPA3	O	GP address line 3
11B	GPA5	O	GP address line 5
12B	GPA6	O	GP address line 6
13B	GPA8	O	GP address line 8
15B	GPA11	O	GP address line 11
16B	GPA13	O	GP address line 13
17B	GPA14	O	GP address line 14
18B	GPD0	I/O	GP data line 0
20B	GPD3	I/O	GP data line 3
21B	GPD5	I/O	GP data line 5
22B	GPD6	I/O	GP data line 6
23B	GPA16	A	GP address line 16
25B	GPA19	O	GP address line 19
26B	GPA21	O	GP address line 21
27B	GPA22	O	GP address line 22
28B	GPD8	I/O	GP data line 8
30B	GPD11	I/O	GP data line 11
31B	GPD13	I/O	GP data line 13
32B	GPD14	I/O	GP data line 14
33B	GPA24	O	GP address line 24
35B	/GPBHE	O	GP Bus Byte High Enable, is active if data is located in the upper 8-bits of the bus
36B	/GPMEMWR	O	GP Bus Memory Write, shows a write access to memory
37B	GPAEN	O	GP Bus Address Enable, shows that the current bus access is a memory access within a DMA cycle
38B	/GPMEMCS16	I	GP Bus Memory Chip Select 16, memory device awaits 16-bit access
40B		-	NC, should remain disconnected
41B	PCI-AD0	I/O	PCI address/data line 0

Pin #	Signal	I/O	Description
Row X1B			
42B	PCI-AD2	I/O	PCI address/data line 2
43B	PCI-AD5	I/O	PCI address/data line 5
45B	PCI-AD7	I/O	PCI address/data line 7
46B	PCI-AD8	I/O	PCI address/data line 8
47B	PCI-AD10	I/O	PCI address/data line 10
48B	PCI-AD13	I/O	PCI address/data line 13
50B	PCI-AD15	I/O	PCI address/data line 15
51B	PCI-AD16	I/O	PCI address/data line 16
52B	PCI-AD18	I/O	PCI address/data line 18
53B	PCI-AD21	I/O	PCI address/data line 21
55B	PCI-AD23	I/O	PCI address/data line 23
56B	PCI-AD24	I/O	PCI address/data line 24
57B	PCI-AD26	I/O	PCI address/data line 26
58B	PCI-AD29	I/O	PCI address/data line 29
60B	PCI-AD31	I/O	PCI address/data line 31
61B	/PCI-RST	O	Reset, serves to reset the attached PCI devices
62B	/PCI-CBE0	I/O	Command or Byte Enable Bus 0
63B	/PCI-CBE3	I/O	Command or Byte Enable Bus 3
65B	/PCI-IRDY	I/O	Initiator Ready, current bus Master has sent data to the bus or is ready to receive data from the bus
66B	/PCI-STOP	I/O	Stop, Target stops current bus transaction
67B	/PCI-REQ0	I	Bus Request, Master 0 wants bus access
68B	/PCI-GNT0	O	Bus Grant 0, bus access released for Master 0
70B	/PCI-REQ2	I	Bus Request, Master 2 wants bus access
71B	/PCI-GNT2	O	Bus Grant 2, bus accessed released form Master 2
72B	/PCI-GNT3	O	Bus Grant 3, bus accessed released for Master 3
73B	/PCI-REQ4	I	Bus Request, Master 4 wants bus access
75B	/PCI-INTB	I	Interrupt Request, PCI Interrupt B
76B	/PCI-INTD	I	Interrupt Request, PCI Interrupt D
77B	/PCI-TRDY	I/O	Target Ready, Target is ready to conclude current data transfer
78B	PCI-CLK1	O	PCI Clock line 1
80B	/PCI_SERR		System error, shows address parity error or other system error, that could be catastrophic

Pin #	Signal	I/O	Description
Row X1C			
1C	VCC2	-	Core operating voltage 2.5 Volts for the processor
2C	VCC2	-	Core operating voltage 2.5 Volts for the processor
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C	GND	-	Ground
4C	VCC5	-	5 Volt operating voltage for SIO and Ethernet controller
5C	VCC5	-	5 Volt operating voltage for SIO and Ethernet controller
6C	VBAT	-	External operating voltage, 3 Volt
8C	NC	-	NC, should remain disconnected
9C	NC	-	NC, should remain disconnected
10C	PWRGOOD	O	Power Good signal, can be used as a reset for the periphery
11C	GPRESET	O	GP Bus Reset, for resetting connected GP Bus devices
13C	SIOGP13	I/O	In-/Output 13 of the SIO device
14C	SIOGP15	I/O	In-/Output 15 of the SIO device, can be configured as an infrared IRTx
15C	SIOGP50	I/O	In-/Output 50 of the SIO device
16C	SIOGP54	I/O	In-/Output 54 of the SIO device
18C	/RTS4	O	Request To Send, COM 4
19C	/DSR4	I	Data Set Ready, COM 4
20C	/DTR4	O	Data Terminal Ready, COM 4
21C	RXD232-2	I	Received Data, COM 2
23C	TXD232-2	O	Transmitted Data COM 2
24C	RTS232-2	O	Request To Send, COM 2
25C	CTS232-2	I	Clear To Send, COM 2
26C	DSR232-2	I	Data Set Ready, COM 2
28C	DTR232-2	O	Data Terminal Ready, COM 4
29C	RIN232-2	I	Ring Indicator, COM 2
30C	DCD232-2	I	Received Line Detector Carrier Detector, COM 2
31C	SSI-CLK	O	SSI interface, clock line
33C	ETH-LINKLED	O	Ethernet Link LED connector
34C	ETH-LANLED	O	Ethernet LAN LED connector
35C	ETH-RXD-	I	Ethernet receive line (negative)
36C	ETH-TXD-	O	Ethernet send line (negative)
38C	PE	I	Paper empty
39C	/INIT	O	Printer initialization
40C	/ACK	I	Data assumed
41C	/SLCTIN	O	Select in, On-Line connection
43C	PD0	O	Parallel data 0
44C	PD2	O	Parallel data 2
45C	PD3	O	Parallel data 3
46C	PD5	O	Parallel data 5
48C	KBDATA	I	Keyboard data line

Pin #	Signal	I/O	Description
Row X1C			
49C	MDATA	I	Mouse data line
50C	MCLK	O	Mouse clock line
51C	TXD3	O	Transmitted data COM 3
53C	/DSR3	I	Data Set Ready, COM 3
54C	/RI3	I	Ring Indicator, COM 3
55C	/DCD3	I	Received Line Detector Carrier Detector, COM 3
56C	DRAT0	O	Drive density select 1
58C	/DS0	O	Drive Select 0
59C	/DIR	O	Step Direction
60C	/STEP	O	Step Pulse
61C	/WGATE	O	Write Gate
63C	/TRACK0	I	Track 0
64C	/RDATA	I	Read Disk Data
65C	/DSKCHNG	I	Disk Change
66C	NC	-	NC, should remain disconnected
68C	/IDE-CS1	O	IDE Chip Select 1
69C	/GPCS6	O	GP Chip Select 6, can address memory or I/O devices or be configured as timer output 1
70C	/GPCS7	O	GP Chip Select 7, can address memory or I/O devices or be configured as timer output 0
71C	GPIRQ9	I	GP Bus Interrupt Request 9 or PIO 14, interrupt input 1 or programmable in-/output 14
73C	/GPDACK0	O	GP Bus DMA Acknowledge, release signal for DMA 0 Request
74C	/GPDACK1	O	GP Bus DMA Acknowledge, release signal for DMA 1 Request
75C	CLKTIMER	I	Timer Clock Input, external clock input for Programmable Interval Timer (PIT)
76C	/ROMBUFOE		ROM Buffer Output Enable, shows access to Flash devices
78C	/FLASHWR	O	Write signal for external Flash devices
79C	/ROMRD	O	Read signal for external Flash devices
80C	CLK32OUT	O	32 kHz clock output

Pin #	Signal	I/O	Description
Row X1D			
1D	VCC2	-	Core operating voltage 2.5 V for the processor
2D	VCC2	-	Core operating voltage 2.5 V for the processor
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D	GND		
4D	VCC3	-	I/O operating voltage 3.3 V for the processor
5D	VCC3	-	I/O operating voltage 3.3 V for the processor
6D	VPD	-	Back-up voltage output 3 V (5 V)
7D	NC	-	NC, should remain disconnected
8D	NC	-	NC, should remain disconnected
10D	/RESETIN	I	External Reset
11D	SIOGP10	I/O	In-/Output 10 of the SIO device
12D	SIOGP12	I/O	In-/Output 12 of the SIO device
13D	SIOGP14	I/O	In-/Output 14 of the SIO device, can be configured as a infrared interface IRRx
15D	SIOGP53	I/O	In-/Output 53 of the SIO device
16D	RXD4-IRDA	I	Received Data, COM 4 or infrared interface IRRx
17D	TXD4-IRDA	O	Transmitted Data COM 4 or Infrared interface IRTx
18D	/CTS4	I	Clear To Send, COM 4
20D	/RI4	I	Ring Indicator, COM 4
21D	/DCD4	I	Received Line Detector Carrier Detector, COM 4
22D	RXD232-1	I	Received Data, COM 1
23D	TXD232-1	O	Transmitted Data COM 1
25D	RTS232-1	O	Request To Send, COM 1
26D	CTS232-1	I	Clear To Send, COM 1
27D	DSR232-1	I	Data Set Ready, COM 1
28D	DTR232-1	O	Data Terminal Ready, COM 1
30D	RIN232-1	I	Ring Indicator, COM 1
31D	DCD232-1	I	Received Line Detector Carrier Detector, COM 1
32D	SSI-DO	O	SSI Interface data output
33D	SSI-DI	I	SSI Interface data input
35D	ETH-RXD+	I	Ethernet receive line (positive)
36D	ETH-TXD+	O	Ethernet send line (positive)
37D	/STRB	O	Strobe, data is valid
38D	BUSY	I	Not ready to receive new data
40D	/AFDT	O	Add an LF for every CR
41D	/ERROR	I	Printer interference
42D	SLCT	I	Select, Printer is online
43D	PD1	O	Parallel data 1
45D	PD4	O	Parallel data 4
46D	PD6	O	Parallel data 6
47D	PD7	O	Parallel data 7
48D	KBCLK	O	Keyboard clock
50D	RXD3	I	Received Data, COM 3

Pin #	Signal	I/O	Description
Row X1D			
51D	/RTS3	O	Request To Send, COM 3
52D	/CTS3	I	Clear To Send, COM 3
53D	/DTR3	O	Data Terminal Ready, COM 3
55D	DRVEN	O	Drive Density Select 0
56D	/MTR0	O	Motor On 0
57D	/MTR1	I/O	Motor on 1
58D	/DS1	I/O	Drive Select 1
60D	/WDATA	O	Write Disk Data
61D	/HDSEL	O	Head Select
62D	/INDEX	I	Index Pulse input
63D	/WRTPRT	I	Write Protected
65D	NC	-	NC, should remain disconnected
66D	NC	-	NC, should remain disconnected
67D	IDE-CS0	O	IDE Chip Select 0
68D	/GPCS5	O	GP Chip Select 5, can address memory or I/O devices or be configured as timer input 0
70D	GPIRQ6	I	GP Bus Interrupt Request 6 or PIO 17, interrupt input 6 or programmable in-/output 17
71D	GPIRQ10	I	GP Bus Interrupt Request 10 or PIO 13, interrupt input 10 or programmable in-/output 13
72D	GPDRQ0	I	GP Bus DMA Request, DMA channel 0 inquiry
73D	GPDRQ1	I	GP Bus DMA Request, DMA channel 1 inquiry
75D	PITOUT2	O	Programmable Interval Timer Output 2, normally a speaker output
76D	PRGRESET	I	Programmable Reset, programmable reset, SDRAM is refreshed again
77D	/POWERON	O	Signal for activation of the adapter
78D	BUTTON-IN	I	In-/Out button connector
80D	VSTDBY	-	5 V Stand-by supply voltage for power management and Ethernet controller (Wake on LAN)

Table 1: Pinout of the phyCORE-Connector X1

2.1 Supply Voltage

The phyCORE-SC520 requires up to three separate supply voltages depending on the level of expansion. These are 2.5 V for the core voltage of the processor, 3.3 V for the I/O voltage of the processor and, if the SIO device (Serial Input/Output device) is connected, an additional 5 V supply. There are multiple pins available for the connection of the individual operating voltages. We highly recommend connecting all available operating voltages and correspond GND pins. Only this will guarantee sufficient current flow and maximized electromagnetic tolerance.

Pin No. at X1	Signal Name
1C, 1D, 2C, 2D	2.5 V (processor core)
4D, 5D	3.3 V (processor I/O)
4C, 5C	5 V (SIO connected) 3.3 V (SIO not connected)
6C	VBAT (ext. 3 V battery input)
6D	VPD (battery voltage output)
80D	VSTDBY 5 V (SIO connected) 3.3 V (SIO not connected)

Table 2: Supply Voltage Connections

VBAT is used to connect an external 3 V battery to maintain the CMOS data and the function of the RTC.

VPD is used to connect the battery voltage (on board battery or external battery) to external peripherals.

VSTDBY is a voltage used for power management. If the SIO device is connected the voltage amounts to 5 V, otherwise it is 3.3 V.

Note:

This voltage must always remain available. If no power management is to be used, the voltage can be connected directly to the corresponding supply voltage.

If the SIO device is not connected, the 5 V operating voltage is not necessary. Instead 3.3 V can be connected to the connectors 4C and 5C. The GP control bus as well as the GP data bus are thereby able to operate with 3.3 V.

The module's current draw is dependent upon the different configuration variations. In the table below the maximum current values are listed. The current of the individual variants must be added to the current of the base module.

Voltage	Base Modul	+ SIO	+ Ethernet
2.5 V	660 mA	-	-
3.3 V	200 mA	-	-
5 V	-	+ 100 mA	-
VSTDBY	1 mA	+ 25 mA	+ 330 mA*
VBAT	5 μ A**	1 μ A	-

Table 3: Current Draw

- The Ethernet controller has no special stand-by voltage input. The stand-by voltage is simultaneously the operating voltage, therefore the stand-by adapter must be appropriately configured.
- If the SIO device is connected, the RTC of the Elan SC520 is disabled, so that only the current draw of the SIO is relevant.

2.2 AMDebug Interface

The phyCORE SC520 has an expanded JTAG (AMDebug) interface defined by AMD. The interface signals are accessible at the edge of the module (X2). If needed a pin header connector in 2 mm pitch can be soldered into solder holes at X2. This allows for direct hardware debugger connection. The required hardware debuggers are available from different vendors.

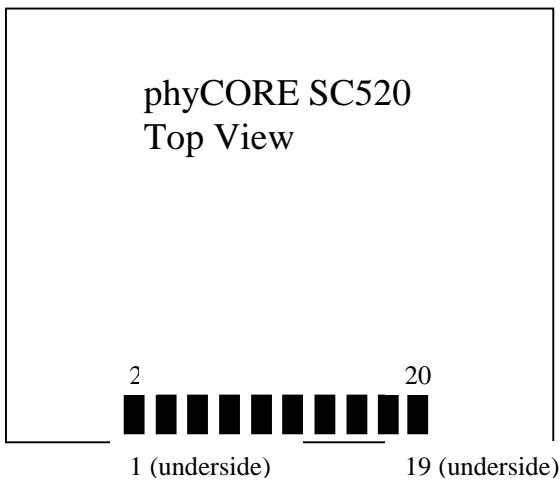


Figure 4: Pinout of the AMDebug-Connector X2

Caution:

All JTAG signals are generated at 3.3 V. Because of their direct connection, an overvoltage could destroy the processor!

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	11	/JTAG_TRST
2	Pwrgood (3,3 V)	12	GND
3	JTAG_TCK	13	/SYSRESET
4	GND	14	GND
5	JTAG_TMS	15	CMDACK
6	GND	16	GND
7	JTAG_TDI	17	BR/TC
8	GND	18	TRIG/TRACE
9	JTAG_TDO	19	STOP/TX
10	GND	20	NC, Key

Table 4: Pinout of the AMDebug-Connector X2

2.3 Serial Interfaces

The phyCORE-SC520 has four serial interfaces, whereby the first two, COM1 and COM2, are made available by the Elan SC520 and the other two COM3 and COM4 are made available by the SIO device. The signal levels of COM1 and COM2 are set to V24 over two RS-232 transceivers, while COM3 and COM4 have a 5 V TTL level. All four interfaces are fully modem capable and can be integrated in power management (WakeOnModem). The exact specifications of the UART can be found in the "*Elan SC520 Microcontroller User's Manual*" from AMD as well as in the documentation for the "*FDC37B787, Enhanced Super I/O Controller with ACPI Support, Real-Time Clock and Consumer IR*" from SMSC.

The serial interface signals are available on the phyCORE-connector X1 (Molex) at the pins as listed in the tables below:

COM1 RS-232/V24 Signal Name	Pin # at X1
RxD232-1	22D
TxD232-1	23D
RTS232-1	25D
CTS232-1	26D
DSR232-1	27D
DTR232-1	28D
RIN232-1	30D
DCD232-1	31D

Table 5: Pinout of the Serial Interface COM1 (V24)

COM2 RS-232/V24 Signal Name	Pin # at X1
RxD232-2	21C
TxD232-2	23C
RTS232-2	24C
CTS232-2	25C
DSR232-2	26C
DTR232-2	28C
RIN232-2	29C
DCD232-2	30C

Table 6: Pinout of the Serial Interface COM2 (V24)

COM3 RS-232/TTL Signal Name	Pin # at X1
RxD3	50D
TxD3	51C
/RTS3	51D
/CTS3	52D
/DSR3	53C
/DTR3	53D
/RI3	54C
/DCD3	55C

Table 7: Pinout of the Serial Interface COM3 (5 V TTL)

COM4 RS-232/TTL Signal Name	Pin # at X1
RxD4_IrDa	16D
TxD4_IrDa	17D
/RTS4	18C
/CTS4	18D
/DSR4	19C
/DTR4	20C
/RI4	20D
/DCD4	21D

Table 8: Pinout of the Serial Interface COM4 (5 V TTL)

Example circuitry for connection can be found in *section 7.6*.

2.4 Infrared Interface

The SIO's UART 2 (COM4) can be reconfigured as an infrared interface. In this configuration, the device supports the following protocols:

- IrDa
- Consumer IR
- HP-SIR and
- ASK-IR.

There are two possibilities of connecting the transmit/receive unit to the phyCORESC520.

- The transmit and receive line of the interface COM4 can be used.
- In addition to this, the signals are also available on the two I/O ports of the SIO device, which extend to the Molex connector at X1.

The interface's UART must be configured appropriately (see "*FDC37B787, Enhanced Super I/O Controller with ACPI Support, Real-Time Clock and Consumer IR*" from SMSC). If the IR transmit/receive unit is connected to the I/O ports, there is the possibility of switching between the "normal" interface and the infrared interface via software, without having to alter cable connections. Example circuitry for connection can be found in *section 7.8*.

IrDa Signal Name	Molex Signal Name	Pin # at X1
IRRX	RxD4_IrDa	16D
IRTX	TxD4_IrDa	17D

Table 9: Pinout IR Interface on COM4 Pins

IrDa Signal Name	Molex Signal Name	Pin # at X1
IRRX	SIOGP14	13D
IRTX	SIOGP15	14C

Table 10: Pinout IR Interface on I/O Pins

2.5 Parallel Interface

The parallel interface is made available by the SIO device. The following modes are supported:

- SPP (Standard Parallel Port)
- Bidirectional Parallel Port (XT, AT, PS/s compatible)
- Enhanced Mode
- EPP (Enhanced Parallel Port), EPP 1.7 and EPP 1.9 (IEEE1284)
- ECP (Extended Capabilities Port)

For configuration of the individual modes refer to "*FDC37B787, Enhanced Super I/O Controller with ACPI Support, Real-Time Clock and Consumer IR*" from SMSC. Example circuitry for connection can be found in *section 7.7*.

Parallel Port Signal Name	Pin # at X1
/STRB	37D
/AFDT	40D
/ERROR	41D
/ACK	40C
BUSY	38D
PE	38C
SLCT	42D
/INIT	39C
/SLCTIN	41C
PD0	43C
PD1	43D
PD2	44C
PD3	45C
PD4	45D
PD05	46C
PD6	46D
PD7	47D

Table 11: Pinout of the Parallel Interface

2.6 Floppy Interface

The SIO device has a floppy disc controller that supports two 2.88 MB floppy-drives. An exact description of its function can be found in "*FDC37B787, Enhanced Super I/O-Controller with ACPI Support, Real-Time Clock and Consumer IR*" from SMSC. Example circuitry for connection can be found in *section 7.3*.

Floppy-Drive Signal Name	Pin # at X1
DRVEN	55D
DRAT0	56C
/MTR0	56D
/MTR1	57D
/DS0	58C
/DS1	58D
/DIR	59C
/STEP	60C
/WDATA	60D
/WGATE	61C
/HDSEL	61D
/INDEX	62D
/TRACK0	63C
/WRTPRT	63D
/RDATA	64C
/DSKCHNG	65C

Table 12: Pinout of the Floppy Interface

2.7 IDE Interface

In addition to the ISA bus signals, two Chip Select signals IDE_CS0 and ICE_CS1 are available for establishing a hard drive connection. If the length of the cable between the phyCORE-SC520 and the IDE device is more than 100 mm we recommend connecting bus drivers to the data lines in order to reduce EMI radiation. Example circuitry for connection can be found in *section 7.2*.

IDE Signal Name	Pin # at X1
IDE_CS0	67D
IDE_CS1	68C
GPIRQ10	71D
GPDRQ1	73D
/GPDACK1	74C

Table 13: IDE-Specific Signals

2.8 Keyboard and Mouse Interfaces

The SIO provides an 8042 keyboard controller for connection of a PS/2 keyboard and a PS/2 mouse. The interface's function is described in "*FDC37B787, Enhanced Super I/O Controller with ACPI Support, Real-Time Clock and Consumer IR*" from SMSC. Example circuitry for connection can be found in *sections 7.4 and 7.5*.

Keyboard Signal Name	Pin # at X1
KBDATA	48C
KBCLK	48D

Table 14: Keyboard Interface

Mouse Signal Name	Pin # at X1
MDATA	49C
MCLK	50C

Table 15: Mouse Interface

2.9 Ethernet Connector

If the optional Ethernet controller RT8139 from Realtec populates the phyCORE-SC520 and a network connection needs to be enabled, a YCL 20PMT04 transmitter must be connected. Example circuitry for connection can be found in *section 7.9*.

Ethernet Signal Name	Pin # at X1
ETH_RXD-	35C
ETH_RXD+	35D
ETH_TXD-	36C
ETH_TXD+	36D
ETH_LINKLED	33C
ETH_LANLED	34C

Table 16: Ethernet Connector

2.10 SSI Interface

The Elan SC520 has a hardware implemented Synchronous Serial Interface (SSI). This interface is suitable for connection of 4-pin as well as 3-pin devices. The connector lines extend to the Molex connector rows. There is a serial EEPROM located on the phyCORE-SC520 that is connected with 4-pin technology, thereby enabling full duplex access. It is important to note that when 3-pin devices are connected, this possibility no longer exists, since in this case the SSI_DI and SSI_DO are connected to each other. Example circuitry for connection can be found in *section 7.1*.

SSI Port Name	Pin # at X1
SSI-CLK	31C
SSI-DO	32D
SSI-DI	33D

Table 17: Pinout of the SSI Interface

2.11 ISA Bus

The SC520 controller features a general purpose bus that replicates a standard PC/AT 16-bit ISA bus according to the configuration in the System-BIOS. The signal lines of the ISA bus extend to the Molex connector. Two of the four DMA channels made externally available by the Elan SC520 are connected to the SIO controller and are therefore no longer available on the pin header rows. The same is true for various interrupt lines: these are partially available on the pin header rows, but are also used by the SIO according to BIOS initialization.

The integrated SIO device runs with an operating voltage of 5 V and is directly connected to the ISA bus. Therefore the data and control bus are both configured at 5 V (the Elan SC520 runs with 3.3 V, however it can tolerate an input voltage of 5 V). The voltage level of the address bus, which is unidirectional, was left at 3.3 V, which is the pre-defined value given by the SC520. The four possible scenarios for connecting external peripherals are as follows:

- 1) A 5 V ISA peripheral device needs to be connected, the address inputs of the external device already function at a high level of 3.3 V (i.e. CMOS).

In this case no additional external circuitry is required, since address, control and data lines can be connected directly.

- 2) A 5 V ISA peripheral device needs to be connected, the address inputs of the external device function at a high level of 5 V (i.e. TTL).

In this case the applicable address lines must be switched to 5 V over a unidirectional transceiver.

Caution:

Do not simply connect pull-up resistors to the address lines! This would cause destruction of the SC520 controller since the address outputs are not 5 V tolerant!

- 3) A 3.3 V ISA peripheral device needs to be attached, the data and control signals of the external device are 5 V tolerant.
In this case no additional external circuitry is required.

- 4) A 3.3 V ISA peripheral device needs to be attached, the data and control signals of the external device are **not** 5 V tolerant.

In this case the level of the control bus lines that are located between the phyCORE-SC520 and the periphery device must be switched to 3.3 V by a voltage level converter. The data bus must be handled individually. Since it functions bidirectionally, a bus driver with direction switching capability must be connected. The outputs of the driver in the direction of the ISA bus can only be enabled if the attached peripheral device actually has data to send to the bus. This can be accomplished with a CS signal and corresponding programming of a PAR register or with external address decoding, that is already available for switching the peripheral devices into the controller's address space.

Note:

Examples for attaching external peripherals to the phyCORE-SC520 can be found in the appendix at the end of this manual.

2.12 PCI Bus

The Elan SC520 controller provides a 33 MHz, 32-bit PCI bus (revision 2.2). Up to 5 bus master can be connected to this PCI bus. The System-BIOS configures the bus for the following PCI slot assignment:

PCI Bus Signal	Slot 1	Slot 2	Slot 3* (VGA)	Slot 4** (Ethernet)
INTA	INTA	INTB	INTC	INTD
INTB	INTB	INTC	INTD	INTA
INTC	INTC	INTD	INTA	INTB
INTD	INTD	INTA	INTB	INTC
REQ0	REQ			
GNT0	GNT			
REQ1		REQ		
GNT1		GNT		
REQ2			REQ	
GNT2			GNT	
REQ3				REQ
GNT3				GNT

Table 18: PCI Bus

* If the phyCORE-SC520 is mounted on the applicable Development Board and the optional VGA controller is populated, then VGA is available as PCI device in slot 3.

** If the optional Ethernet controller populates the phyCORE-SC520, then the Ethernet interface is available as PCI master in slot 4.

If Ethernet and/or VGA controller are not available on the target system the corresponding PCI slots can be used for connecting other devices.

3 System Configuration

The System-BIOS configures the registers of the Elan SC520 and the SIO device so that the phyCORE-SC520 functions like a PC/AT. The following system settings are based on this configuration:

3.1 Memory Mapping

Address Range	Resource
000000....9FFFFh	Low Memory Area
A0000h...BFFFFh	Video Adapter
C0000h...DEFFFh	Adapter-BIOS Extensions
DF000h...DFFFFh	MMCR alias (Real Mode access)
E0000h....EFFFFh	System-BIOS extensions
F0000h....FFFFFh	System-BIOS
100000h.....	High Memory Area
FFFEF000h....FFFEFFFFh	MMCR (Protected Mode access)
FFFFFF000h....FFFFFFFh	Boot Vector BIOS-ROM

Table 19: Memory Mapping

The **Memory Mapped Configuration Region (MMCR)**, shaded in gray in the table above, plays an important role. This region is 4 kBytes in size and contains various configuration and control registers of the Elan SC520. It starts at address FFFE000h. This allows this region to also be addressed in Real Mode the Elan SC520 offers the possibility of accessing this region via a user defined address in the **Configuration Base Address Register (CBAR)**. The BIOS sets the Real Mode start address for this region at DF000h. Access to the MMCR register is now possible in the region FFFE000h....FFFEFFFFh (Protected Mode), as well as in the region DF000h....DFFFFh (Real Mode).

3.2 Interrupts

The programmable interrupt controller of the Elan SC520 consists of three cascaded standard interrupt controllers that have flexible inputs to which various interrupt sources can be connected (*see Elan SC520 Microcontroller User's Manual*). The System-BIOS configures the interrupt controller in accordance to the PC/AT specifications. This results in the following interrupt configuration:

Interrupt Vector Address	Priority	Name	Standard Interrupt Source (responsible device)
08h	1	IRQ 0	System Timer (SC520)
09h	2	IRQ 1	Keyboard (SIO)
0Ah	---	IRQ 2	Cascading (SC520)
0Bh	11	IRQ 3	COM2 (SC520)
0Bh	11	IRQ 3	COM4 (SIO)
0Ch	12	IRQ 4	COM1 (SC520)
0Ch	12	IRQ 4	COM3 (SIO)
0Dh	13	IRQ 5	Free
0Eh	14	IRQ 6	Floppy (SIO)
0Fh	15	IRQ 7	LPT1 (SIO)
70h	3	IRQ 8	RTC (SIO)
71h	4	IRQ 9	Free
72h	5	IRQ 10	Free
73h	6	IRQ 11	Power Management (SIO)
74h	7	IRQ 12	Mouse (SIO)
75h	8	IRQ 13	Coprocessor (SC520)
76h	9	IRQ 14	Hard-drive (GPIRQ 10)
77h	10	IRQ 15	Free

Table 20: *Interrupt Configuration*

The following interrupt lines are available on the Molex connectors:

Interrupt Name at Molex Connector X1	Interrupt Vector Address	Priority	Name
GPIRQ 0 (Molex pin 2B)	74h	7	IRQ 12
GPIRQ 1 (Molex pin 3A)	09h	2	IRQ 1
GPIRQ 2 (Molex pin 3B)	72h	5	IRQ 10
GPIRQ 3 (Molex pin 65D)	0Bh	11	IRQ 3
GPIRQ 5 (Molex pin 4A)	0Dh	13	IRQ 15
GPIRQ 6 (Molex pin 70D)	0Eh	14	IRQ 6
GPIRQ 7 (Molex pin 66D)	0Fh	15	IRQ 7
GPIRQ 8 (Molex pin 66C)	70h	3	IRQ 8
GPIRQ 9 (Molex pin 71C)	73h	6	IRQ 11
GPIRQ 10 (Molex pin 71D)	76h	9	IRQ 14

Table 21: Interrupts on the Molex Connector X1

The interrupt sources that are shaded gray in the table above are reserved for the SIO and IDE hard-drive in a normal case, however they also extend to the Molex connectors. An alternative usage for these interrupts requires a reconfiguration of the SIO device (the corresponding SIO connector must be configured as an input, see the Data Sheet for the FDC37B787), however this can easily be accomplished with user software.

If no PCI is used, the four PCI interrupt lines PCI-INTA – PCI-INTD are available on the Molex connector. However the Elan SC520 must be configured accordingly for this purpose (*see Elan SC520 Microcontroller User's Manual*).

3.3 DMA Channels

The Elan SC520 microcontroller is equipped with a DMA controller, that allows for a direct data transfer between the GP bus and SDRAM. It consists of two 4-channel DMA controllers, that can be cascaded (see *Elan SC520 Microcontroller User's Manual*). The System-BIOS configures the DMA channels in PC/AT format as shown below:

DMA Channel	DMA Source	Function
DMA 0	SC520	DRAM Refresh
DMA 1	Molex (GPDRQ1)	Hard-Drive
DMA 2	SIO	Floppy
DMA 3	SIO	Parallel port
DMA 4	SC520	Cascading
DMA 5	Molex (GPDRQ0)	Free
DMA 6		Unused
DMA 7		Unused

Table 22: DMA Connections

3.4 Chip Select Signals

The Elan SC520 microcontroller provides 9 Chip Select signals. Each individual signal can be either mapped to the controller's I/O address area or in a memory address area. The Chip Select signals can be configured over the **Programmable Address Region (PAR)** register in the SC520 (see *Elan SC520 Microcontroller User's Manual*). The System-BIOS configures the Chip Select signals for access to the Flash device and the hard-drive. All additional Chip Select signals can be freely programmed with the help of the PAR register.

Chip Select	Address Range	Function
/BOOTCS	00000h...FFFFFh 8000000h – 8FFFFFFh	Flash device
/GPCS0	1F0h - 1F7h	IDE CS0
/GPCS1		Free
/GPCS2		Free
/GPCS3	3F6h – 3F7h	IDE CS1
/GPCS4		Free
/GPCS5		Free
/GPCS6		Free
/GPCS7		Free

Table 23: Chip Select Configuration

3.5 Programmable Address Region Register

In order to enable access to various I/O and memory address areas, the Elan SC520 is equipped with 15 configuration registers. With these registers the address space of the SC520 is configured and access to the peripheral devices is defined. The System-BIOS configures parts of the registers so that a PC/AT compatible memory model and I/O model is established.

Name	Address Range	Access Type	Function
PAR 0	A0000h..BFFFF	Memory	PCI Video Memory
PAR 1			Not used
PAR 2	1F0h...1F7h	I/O	IDE CS0
PAR 3	3F6h...3F7h	I/O	IDE CS1
PAR 4			Not used
PAR 5	A0000h...BFFFFh	Memory	ISA Video Memory
PAR 6	C0000h...C7FFFh	Memory	ISA VGA BIOS
PAR 7	46E8h	I/O	ISA VGA Initialization
PAR 8	8000000h..8FFFFFFh	Memory	Flash Device
PAR 9			Not used
PAR 10	C8000h...DF000h	I/O	ISA
PAR 11	C8000h...DF000h	I/O	ISA
PAR 12	C8000h...DF000h	I/O	ISA
PAR 13			Not used
PAR 14			Reserved (BIOS)
PAR 15	E0000...FFFFFF	Memory	Reserved (BIOS)

Table 24: PAR Register Configuration

3.6 SIO Initialization

The SIO device is attached to the ISA bus (8-bit data bus width) and its interrupt request outputs and DMA lines are directly connected to the corresponding inputs of the SC520 (see circuit diagram). Access to the SIO device is possible at address 3F0h (CONFIG PORT) and 3F1h (INDEX PORT) in case additional programming is required (refer to the "FDC37B787, Enhanced Super I/O Controller with ACPI Support, Real-Time Clock and Consumer IR" Data Sheet).

The System-BIOS configures the SIO device so that the available hardware expansions are PC/AT conformant. This means that standard AT addresses, interrupts and DMA channels are used.

Device	Addresses	IRQ Pin SIO	DMA Pins SIO
Floppy	3F0h-3F7h	IRQ 6	DRQ2, /DACK2
Parallel Port	378h	IRQ 7	DRQ3, /DACK3
COM3	3E8	IRQ 4	-
COM4	2E8	IRQ 3	-
Keyboard	60h, 64h	IRQ1	-
Mouse		IRQ15	-
RTC*	70h, 71h	IRQ8	-
Power Management		IRQ9	-

Table 25: Super I/O Interrupt and DMA Configuration

* The RTC integrated in the SIO device is used rather than the RTC in the Elan SC520. The RTC of the SIO draws less current and can be included in the integrated power management.

4 System-BIOS

The System-BIOS from General Software was adapted by PHYTEC to the special features of the Elan™SC520, whereby the Power-Down modes were taken into consideration as well. All BIOS interrupts available on desktop PC's (or compatible machines) are supported.

The phyCORE-SC520 is populated with Flash memory in which the System-BIOS (128 kByte) as well as the image of the Flash drive is accommodated. The System-BIOS copies itself into the address region E0000h-FFFFh of the DRAM (shadow-RAM-region) during the Boot procedure.

4.1 Various Boot Modes

The SC520 reads the signals RSTLD0 – RSTLD7 (GPA15 – GPA22) after a hardware reset and stores their values in a register. The System-BIOS uses this characteristic in order to give the user the possibility of booting in various ways.

The following possibilities are available:

1. Normal Mode (RSTLD0... RSTLD2=0)
The BIOS boots until the operating system is prompted. If no graphic card is present, the inputs and outputs are redirected to the serial interface COM1. Thus the boot procedure can be observed and influenced via a connected PC with a terminal program.
2. Safe Mode (RSTLD0=1)
The BIOS values are set back to their factory default settings and the boot procedure starts without shadowing.
3. Manufacturing Mode (RSTLD1=1)
The boot procedure directly starts the manufacturing mode. This means that communication with the phyCORE-SC520 can begin immediately over the corresponding interface.

4. No redirection (RSTLD2=1)

No outputs are redirected to the serial interface during the boot procedure.

Should any of these possibilities be implemented in the user application, a DIP switch or jumper should be attached to the carrier board.

4.2 CMOS Setup

The COMS setup parameters can be set with the help of the utility that is integrated into the System-BIOS. This COMS setup is invoked if the key is pressed during the memory test immediately after the phyCORE-SC520 is powered on or reset. If the input/output is redirected to the serial interface COM1 (no graphic card present), then the key combination ^C (STRG+C) must be used on a terminal program on the connected PC.

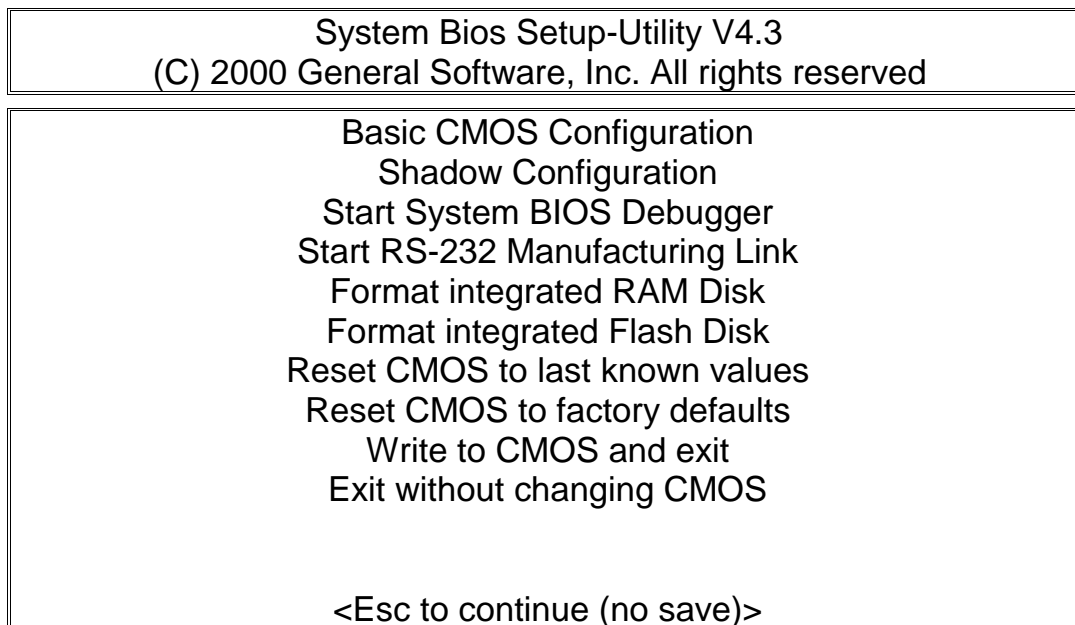


Figure 5: System BIOS Setup-Utility Window

The <TAB> key is used to select the desired subprogram or configuration program within this main menu. Start the selected subroutine by pressing the <Enter> key.

After modifying one or more configurations use the line "Write to CMOS and exit" to exit the System-BIOS CMOS setup.

4.3 Flash Disk

In addition to the BIOS, the Flash device also contains a Flash disk. This means that the memory areas not already occupied by the BIOS itself is addressed and managed like a floppy-drive. The size of this disk depends on the populated Flash device. In order to set up the Flash disk follow the procedure below:

1. Press or <Strg+C> during the boot procedure.
2. Select the menu option *"Basic CMOS Configuration"*
3. Under Drive A: configuration select the Flash disk according to the populated Flash memory device. For example; 917 kByte if a 1 MB Flash device is installed. If a larger Flash populates the phyCORE-SC520 it is possible to set up multiple Flash disks.
4. If the Flash disk is intended to be used as Boot option, drive A: must be set as the first boot selection.
5. At the end of the configuration process press <ESC> to return to the main menu. Here select the menu option *"Write to CMOS and exit"* to save this setting.
6. During the boot procedure press or <Strg+C> again and select *"Format integrated Flash disk"* from the BIOS Setup main menu.
7. Begin formatting by pressing the <Y> key.
8. If data is to be written to the disk, the menu option *"Start RS232 Manufacturing Link"* must be selected from the main menu. Now the phyCORE-SC520 is ready to receive and send data over the serial interface. An exact description can be found in *section 4.4 "Manufacturing Mode"* of this manual.

Caution:

When setting up a Flash disk, the lowest available drive letter must be applied. A:, B:, C:, and D: are valid.

4.4 Manufacturing Mode

The manufacturing mode is an operating mode made available by the System-BIOS that allows the user to access the phyCORE-SC520 and its on-board Flash device over a serial interface. This requires that a host-PC must be connected with the module's COM1 interface via a serial interface cable. In order to render the phyCORE-SC520 into manufacturing mode proceed according to the steps described below:

1. Hit on a connected keyboard during the boot procedure or the use the key combination <Strg+C> if the input/output redirection feature is used in order to get to the BIOS setup main menu.
2. Select the menu option "*Start RS-232 Manufacturing Link*".

The two possible ways on how to access the phyCORE SC520 in manufacturing mode are described below.

4.4.1 Access to Drives Configured in the BIOS (i.e. Flash Disk)

A special DOS driver must be installed and loaded on the host-PC in order to allow access to the various drives installed on or connected to the phyCORE-SC520. This DOS driver is called *mfgdrv.sys* and is located on the Spectrum CD in the folder ...*Tools\Mfg Mode Driver*\\. After installing the driver on the host-PC hard-drive the *mfgdrv.sys* must be loaded with a DEVICE instruction that must be included in your *config.sys* file. This will create a new drive letter on the host-PC. This new drive corresponds with the corresponding drive media on the phyCORE-SC520 indicated in the DEVICE statement of your *config.sys* file.

1. Copy *mfgdrv.sys* from the folder ...*Tools\Mfg Mode Driver* to the hard-drive of the host PC (for example use the DOS folder as destination).
2. Open the *config.sys* file on your hard-drive with an editor program.
3. The following entries should be added or changed:

```
FILES=150  
BUFFERS=15,0  
DEVICE=C:\.....\mfgdrv.sys /BAUD=38K /PORT=COM1 /UNIT=0
```

The entries have the following meanings:

C:\.....\	path to the driver folder
/BAUD	required baud rate
/PORT	desired interface on the host-PC
/UNIT	number of the drive on the phyCORE-SC520 that will be accessed

The baud rate used by the phyCORE-SC520 in manufacturing mode is set at 38,400 baud and can not be changed.

Only the first two serial interfaces COM1 and COM2 are supported by the device driver.

The assignment of numbers to drive letters is arranged as follows:

In case a “soft“ disk is accessed, such as floppy or Flash disk, then the following assignment applies:

/UNIT=0	Drive A:
/UNIT=1	Drive B:
/UNIT=2	Drive C: , no hard drive!
/UNIT=3	Drive D: , no hard drive!

In case a “hard“ disk is accessed, such as hard-disk or Compact Flash card disk, then the following assignment applies:

/UNIT=80 Drive C:

/UNIT=81 Drive D:

If access to multiple drives of the phyCORE-SC520 is desired, the driver must be loaded multiple times accordingly.

Example:

```
DEVICE=C:\.....\mfgdrv.sys /BAUD=38K /PORT=COM1 /UNIT=0  
DEVICE=C:\.....\mfgdrv.sys /BAUD=38K /PORT=COM1 /UNIT=80
```

The first driver addresses Drive A: on the phyCORE-SC520. This drive is either a floppy disk or a Flash disk drive. The drive letter, under which the drive can be addressed on the host-PC, depends on the number of drives installed there. If the last installed drive on the host-PC has the drive letter C:, the drive letter for the remote drive on the phyCORE-SC520 would be D:.

The second driver addresses Drive C: on the phyCORE-SC520. This drive is either a hard drive or a Compact Flash card. The drive letter of this device on the host PC is one letter higher than the previous one, in this case E:.

The procedure described above result that Drive A: of the phyCORE-SC520 can be addressed under the letter D: on the host-PC and that Drive C: of the phyCORE-SC520 can be addressed under the letter E: on the host-PC.

4.4.2 Direct Access to the Flash Device

The program *Flashprg.exe*, contained on the CD, offers the possibility of programming or performing a binary readout of the Flash device. One property of Flash devices is that individual bits can be programmed but not erased. Only entire sectors can be erased. Some Flash devices consist of a specific number of equal sized sectors, others, the boot block types, have various sized sectors at the beginning (boot block bottom type) or at the end (boot block top type) of the device. Boot block top Flash types are populated on the phyCORE-SC520. The sector addresses and sizes depend on this type. The Flash device can be found on the top side of the module, above the processor next to the two RAM devices. The following types are implemented (as of the printing of this manual):

(AM)29LV800BT	(1 MB Flash device)
(AM)29LV160BT	(2 MB Flash device)
(AM)29DL323CT	(4 MB Flash device)

The data sheets of the Flash devices along with sector descriptions are located on the product CD in the folder *Datasheets\Flashes*

Important:

The following sectors contain the System-BIOS and must **NOT** be erased:

(AM)29LV800BT	(1 MB Flash device)
Sector	E0000
Sector	F0000
Sector	F8000
Sector	FA000
Sector	FC000

(AM)29LV160BT (2 MB Flash device)
Sector E0000
Sector F0000
Sector 1E0000
Sector 1F0000
Sector 1F8000
Sector 1FA000
Sector 1FC000

(AM)29DL323CT (4 MB Flash device)
Sector E0000
Sector F0000
Sector 3E0000
Sector 3F0000
Sector 3F2000
Sector 3F4000
Sector 3F6000
Sector 3F8000
Sector 3FA000
Sector 3FC000
Sector 3FE000

It is important to make sure that the addresses that are located outside the address space of the populated Flash device still address the Flash device. This is because the upper address lines are virtually „cut off“. For example, the addresses 1E0000 and 2E0000, in the case of a 1 MB device, will address the sector E0000, which is in fact a BIOS sector. By erasing one of these „mirrored“ sectors the BIOS is also inadvertently erased! Therefore it is important never to address higher addresses than those supported by the populated Flash device!

Note:

With the program *Flashprg.exe* every sector of the Flash device can be erased and overwritten, including the BIOS sectors! Should the BIOS be erased, there is no possibility of restoring it and it is necessary to return the phyCORE-SC520 for repair.

In order to work with the program *Flashprg.exe* the following steps are required:

1. The phyCORE-SC520 must be booted in Manufacturing Mode first (RSTLD1=1, refer to section 4.4). Now the communication with the host-PC can be established via the corresponding interface.
2. Copy *Flashprg.exe* and *Flashprg.bat* from the folder ...*Tools\Flashprg*\ to the hard-drive of the host-PC.
3. Open the file *Config.sys* in the root folder of the hard-drive with an editor.
4. Add or modify the following entries:

```
FILES=150  
BUFFERS=15,0
```

5. Open the file *Flashprg.bat* for editing. Check to see that the baud rate and the interface are set correctly.

Note:

The program *Flashprg.exe* only supports the first two interfaces COM1 and COM2! In *Flashprg.bat* a baud rate of 38 K and COM1 are pre-configured.

6. Now execute the program *Flashprg.bat*. This starts the program *Flashprg.exe* with the configured parameters.
7. In the menu that appears next select the option "*Get Target Attention*" in order to check whether the connection could be established. If this command was successful you will receive the message "*Target Responding*". If no connection could be established you have to check the interface connection and the program prompt.

Read sectors:

1. Select the menu option "*Copy Flash to File*". In the window that appears next, the file name „*Flash.dat*“ will be suggested.
2. By pressing the <TAB> key you can navigate to the next field. All values to be filled in for the fields must be given in hexadecimal format. There the start address of the desired sector is specified. For example, reading out the BIOS enter sector address E0000.
3. By pressing the <TAB> key once more you will get to the field "*Bytes to Copy*". Here enter the desired number of data bytes to be copied. For example, reading out the BIOS enter the hex value "20000" as the BIOS is 128 kBytes in size.
4. Press the <F1> key to start the Flash read procedure. After it is complete you will receive the message "*Flash data written to File*". With <ESC> you can now exit the program. You can view the binary data file with an editor. For example, after reading out the BIOS you will find the BIOS build date and the General Software Copyright message beginning at the 17th data byte.

Erase sector:

1. Select the menu option "*Erase Flash Block*".
2. In the window that appears next enter the start address of the sector that will be erased.
3. Press the <F1> key to begin the erase procedure. After it is complete you will receive the message "*Block erased*".

Program sector:

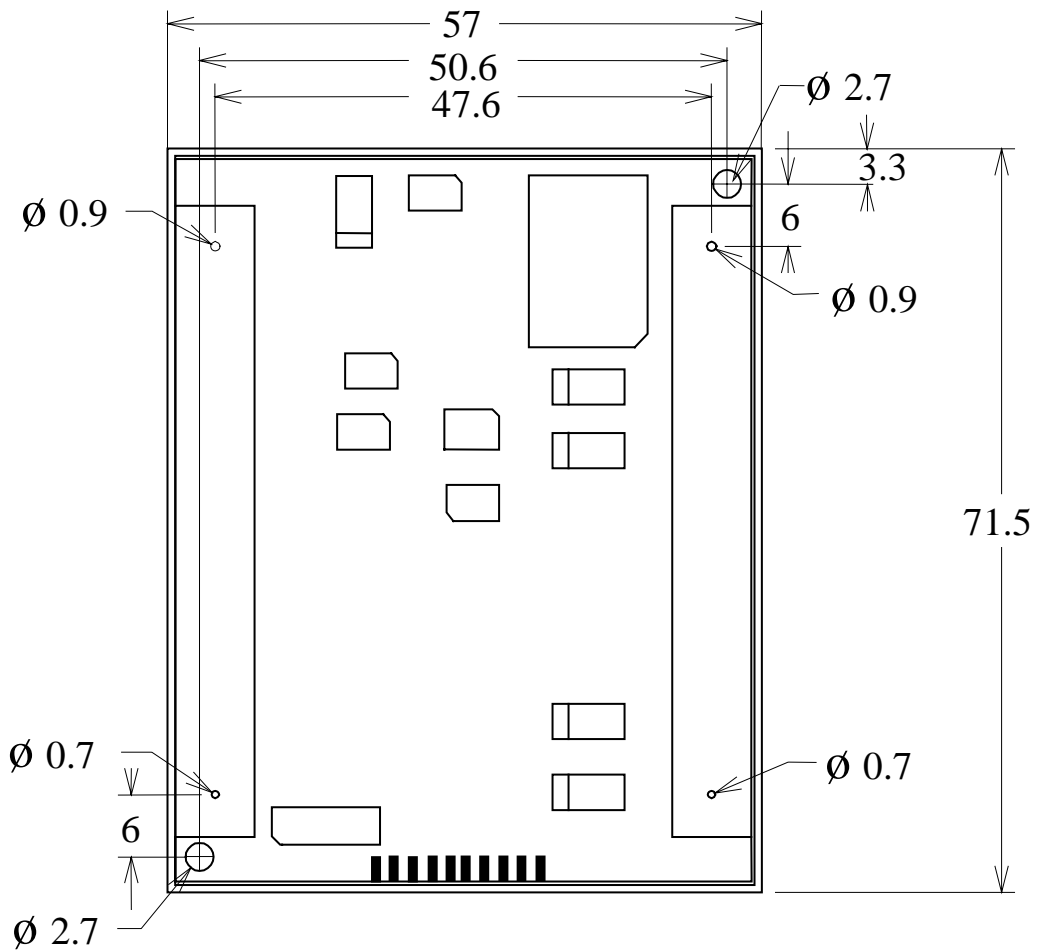
Note:

Before you can program a sector, it must be erased!

1. Select "*Copy File to Flash*". In the window that appears next enter the file name of the binary file to be programmed.
2. Under the menu option "*Hex Flash Offset*" enter the start address of the sector to be programmed.
3. Press the <F1> key to start the programming procedure. After it is complete you will receive the message "*Flash updated*". With <ESC> you can now exit the program.

5 Technical Specifications

The phyCORE-SC520 is shown in its physical dimensions in *Figure 6*. The module profile without pin header rows is approximately 6 mm. The components populated on the underside of the board make up approximately 4.0 mm of this and the components on the top of the board approximately 3.0 mm. The board itself is approximately 1.0 mm thick.



All measurements are in mm

Figure 6: Physical Dimensions

Additional specifications:

- Module Dimensions: 71.5 mm x 57 mm
- Weight: approximately 30 g with all optional components mounted on the board
- Storage Temperature : -40 °C to +90 °C
- Operating Temperature : Standard: 0 °C to +70 °C
Extended: -40 °C to +85 °C
- Humidity: max. 95% r.F. not condensed
- Operating Voltage: 5 V 5 %, 3.3 V 5 %, 2.5 V 5%,
VBAT 3 V 20 %
- Power consumption:

	Min.	Typ.	Max.
2.5 V		465 mA	660 mA
3.3 V		100 mA	120 mA
5 V*		80 mA	100 mA
VSTDBY*	5 mA	25 mA	360 mA
VBAT*	1 µA		5 µA

* depends on the current module option

These specifications describe the standard configuration of the phyCORE-SC520 as of the printing of this manual.

6 Hints for Handling the phyCORE-SC520

Removal and exchange of components on the phyCORE-SC520 is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

7 Connection Examples for External Periphery

The following sections contain examples on how to connect various interfaces and peripheral components to the phyCORE-SC520 with user circuitry. The given examples are intended as guidelines for integrating the phyCORE module into a target application. However, the actual user circuitry may differ from the examples below depending on the specific application requirements. Additional examples and connectivity hints can also be found on the phyCORE Development Board SC520 which is included in the phyCORE-SC520 Development Kit.

7.1 Connecting a Serial Device to the SSI Bus

7.1.1 3-Wire Connection

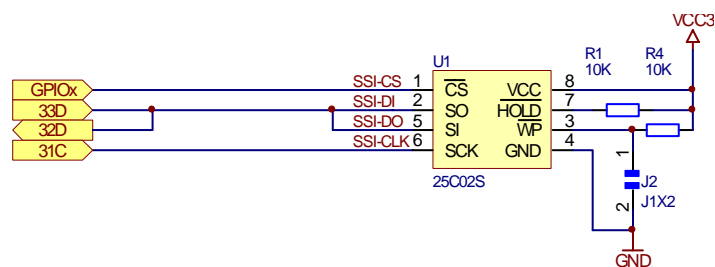


Figure 7: SSI Bus, 3-Wire Connection (Example)

7.1.2 4-Wire Connection

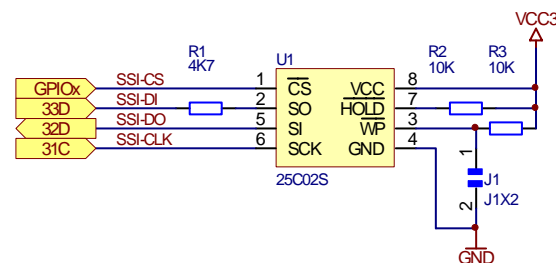


Figure 8: SSI Bus, 4-Wire Connection (Example)

7.2 Connecting a Hard-Drive

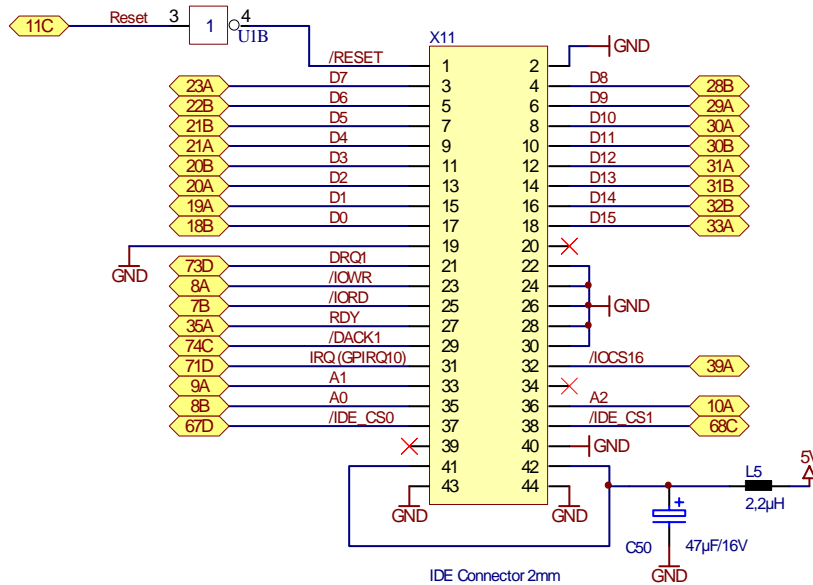


Figure 9: Connecting a Hard-Drive (Example)

7.3 Connecting a Floppy-Drive

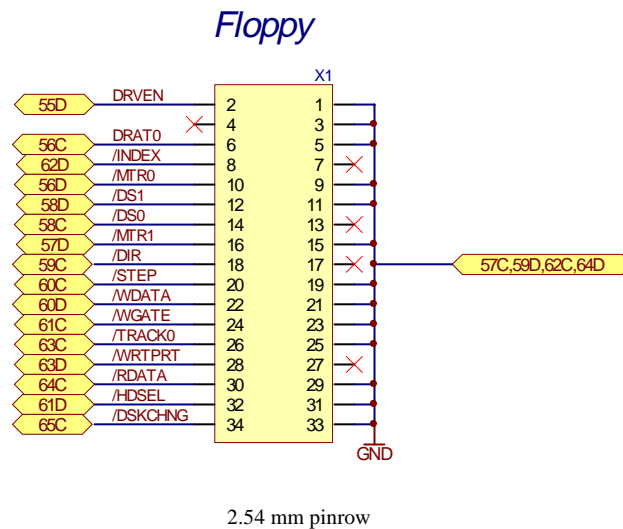


Figure 10: Connecting a Floppy-Drive (Example)

7.4 Connecting a Keyboard

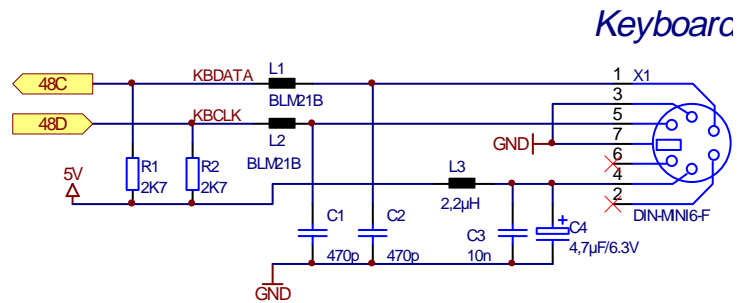


Figure 11: Connecting a Keyboard (Example)

7.5 Connecting a Mouse

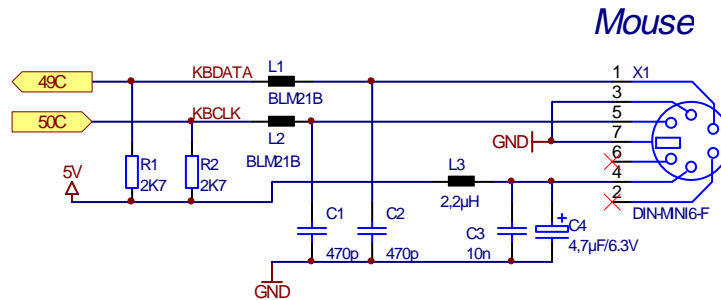


Figure 12: Connecting a Mouse (Example)

7.6 Connecting the Serial Interfaces

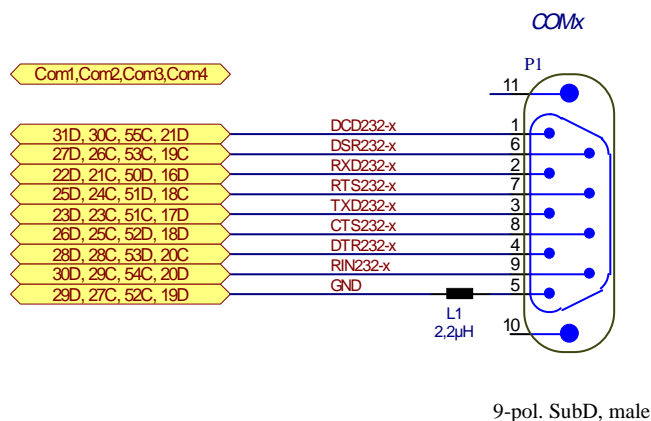
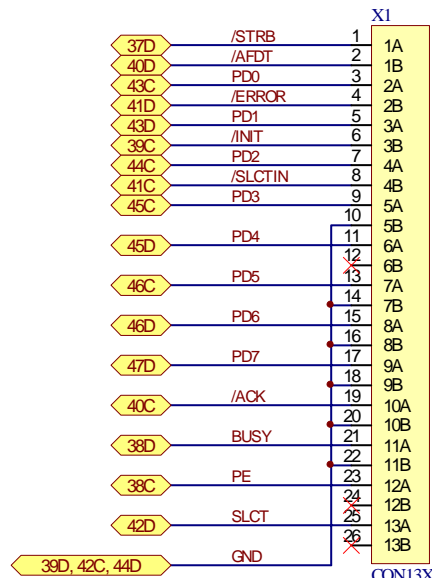


Figure 13: Connecting the Serial Interfaces COMx (Example)

7.7 Connecting the Parallel Interface

Parallel-Port



2.54 mm pin header

Figure 14: Connecting the Parallel Interface (Example)

7.8 Connecting an Infrared Transmit/Receive Unit

7.8.1 Connection at COM4 Pins

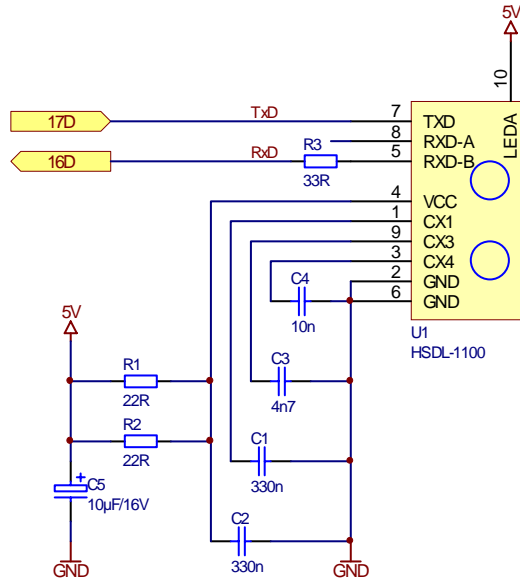


Figure 15: Connecting an Infrared Module (Example with COM4 Pins)

7.8.2 Connecting at SIO GP Pins

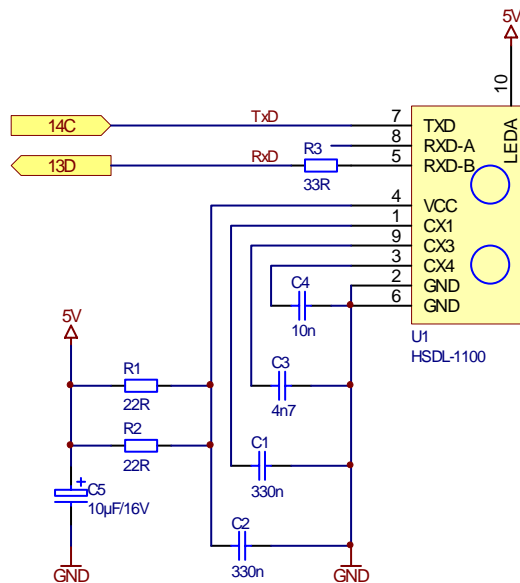


Figure 16: Connecting an Infrared Module (Example with SIO GP Pins)

7.9 Ethernet Connection

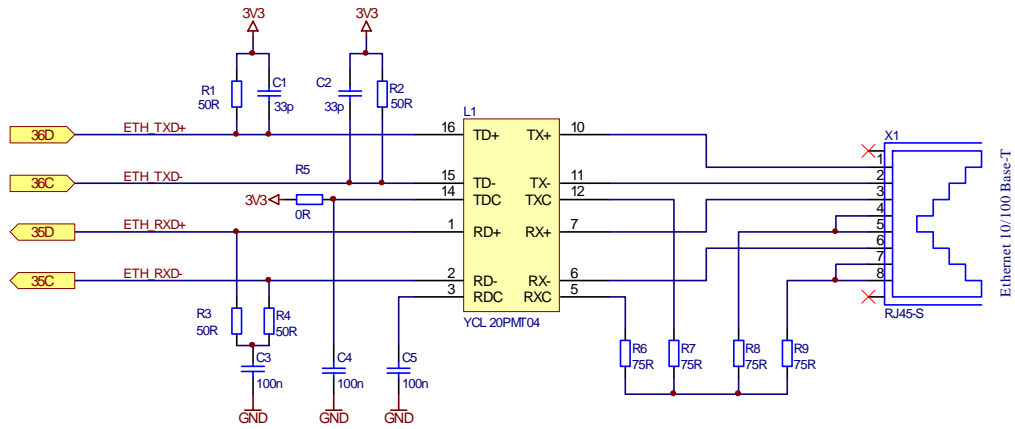


Figure 17: Ethernet Connection (Example)

7.10 Connecting the Boot Jumper

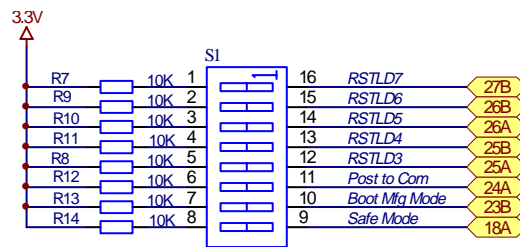


Figure 18: Connecting the Boot Jumper (Example)

Index

2		E	
2.5 V	20	EMC	1
3		Ethernet	64
3.3 V	20	Ethernet Connector.....	29
5		F	
5 V	20	FDC37B787.....	23, 35
8		Features	5
8042.....	28	Flash Disk.....	44, 46
A		Flash Drive	41
Accessing the Flash.....	49	Flashprg.exe	49
AMDebug Interface	22	Floating Point Unit	5
B		Floppy-Drive	27, 60
BIOS.....	50	Floppy Interface	27
BIOS Interrupts	41	H	
Boot Jumper	64	Hard-Drive.....	60
Boot Modes	42	Hints for Handling the	
C		phyCORE-SC520.....	57
CBAR.....	33	Humidity.....	56
Chip Select Signals	37	I	
CMOS Setup	43	IDE	35
COM1.....	23	IDE Interface	28
COM2.....	23, 24	Infrared Interface.....	25, 63
COM3.....	23, 24	Interrupt.....	34
COM4.....	23, 24, 25	Interrupt Configuration	34
Current Draw	21	Introduction	3
D		IrDa.....	25
DMA	36	ISA Bus	30
DMA Channels.....	36	J	
DRAM.....	41	JTAG	22

K		RT8139.....	29
Keyboard.....	61		
Keyboard Interface.....	28		
M		S	
Manufacturing Mode	45	Serial EEPROM	29
Memory Mapping	33	Serial Interfaces.....	23, 61
MMCR.....	33	SIO	25, 26, 27, 28, 30, 35
Module Dimensions	56	SIO Initialization.....	39
Mouse.....	61	SIO Supply	20
Mouse Interface	28	SMT Connector.....	9
O		SSI Interface.....	29, 59
Operating Temperature	56	Storage Temperature	56
Operating Voltage	56	Super I/O Controller.....	23
P		Super-IO.....	39
PAR.....	37	Supply Voltage.....	20
Parallel Interface	26, 62	Synchronous Serial Interface	29
PC/AT	34	System Configuration.....	33
PCI Bus	32	System-BIOS.....	41, 42
PCI Interrupts.....	35	T	
phyCORE-connector.....	9	Technical Specifications	55
Physical Dimensions	55	TTL Level	23
Pin Description.....	9	U	
Pinout	19, 22	UART.....	25
Power Consumption.....	56	V	
Power Management	23	VBAT.....	20
Programmable Address		VPD.....	20
Region.....	37, 38	VSTDBY	20
PS/2.....	28	W	
R		Weight.....	56
RS-232 Transceiver	23	X	
RSTLDx.....	42	X2.....	22

Document: phyCORE-SC520
Document number: L-554e_2, June 2002

How would you improve this manual?

Did you find any mistakes in this manual? _____ page

Submitted by:

Customer number: _____

Name: _____

Company: _____

Address: _____

Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

Published by

PHYTEC

© PHYTEC Meßtechnik GmbH 2002

Ordering No. L-554e_2
Printed in Germany