X-Arc – Embedded Bus *by* PHYTEC

Mit den neuen phyCARD-Produkten hebt PHYTEC die Grenze zwischen Controller und Prozessor auf. Ein neuer Embedded Bus Standard, „X-Arc" (Cross Architecture), macht dies möglich. Hier ist die Pinbelegung.

Signal	Pin		Pin	Signal
VCC	1A		1B	VCC
VCC	2A		2B	VCC
VCC	3A		3B	VCC
GND	4A		4B	GND
VCC_LOGIC	5A		5B	VCC_LOGIC
FEEDBACK	6A		6B	VBAT
nRESET_IN	7A		7B	nRESET_OUT
GND	8A		8B	GND
LVDS_TX0+	9A		9B	LVDS_TX1+
LVDS_TX0-	10A		10B	LVDS_TX1-
LVDS_TX2+	11A		11B	LVDS_TX3+
LVDS_TX2-	12A		12B	LVDS_TX3-
GND	13A		13B	GND
LVDS_TXCLK+	14A		14B	LVDS_CAM_RX+
LVDS_TXCLK-	15A		15B	LVDS_CAM_RX-
LVDS_CAM_MCLK	16A		16B	LVDS_CAM_nLOCK
I2C_CLK	17A		17B	I2C_DATA
GND	18A		18B	GND
ETH_SPEED	19A		19B	ETH_LINK
ETH_TX+	20A		20B	ETH_RX+
ETH_TX-	21A		21B	ETH_RX-
GND	22A		22B	GND
USB_PWR1	23A		23B	USB_PWR2
USB_OC1	24A		24B	USB_OC2
GND	25A		25B	GND
USB_VBUS1	26A		26B	USB_VBUS2
USB_D1-	27A		27B	USB_D2-
USB_D1+	28A		28B	USB_D2+
USB_UID1	29A		29B	USB_UID2
GND	30A		30B	GND
SDIO_D0	31A		31B	SDIO_D1
SDIO_D2	32A		32B	SDIO_D3
SDIO_CLK	33A		33B	SDIO_CMD
GND	34A		34B	GND
SPI_CS0	35A		35B	SPI_CS1
SPI_RDY	36A		36B	SPI_MOSI
SPI_CLK	37A		37B	SPI_MISO
GND	38A		38B	GND
UART_TXD	39A		39B	UART_RXD
UART_RTS	40A		40B	UART_CTS
GND	41A		41B	GND
HDA_BITCLK	42A		42B	AC97_CLK
AC97/HDA_SDATA_OUT	43A		43B	AC97/HDA_SYNC
AC97/HDA_SDATA_IN	44A		44B	AC97/HDA_nRESET
GND	45A		45B	GND
GPIO0/IRQ	46A		46B	GPIO1/IRQ
GPIO2/IRQ	47A		47B	RFU
RFU	48A		48B	RFU
GND	49A		49B	GND
CONFIG0	50A		50B	CONFIG1