## Deltasheet phyCORE-MPC5200B-tiny Circuit Board Revision Update 1245.0 to 1245.1

1. Flash

• Flash connection in 16-bit multiplexed mode

The connection of the Flash devices to the LocalPlus bus using a 16-bit data bus multiplexed mode allows populating future Flash devices with up to 32 Mbyte capacity on the phyCORE module. This bus access mode needs to be considered when developing software drivers for Flash access (such as MTD driver for example).

- 2. Ethernet (precise name: Ethernet PHY):
  - PHY U2 is being replaced by the KSZ8001LI

This makes a separate PHY-RESET input available on the Molex connector (pin 8D). The PHY can now be reset via the /Hreset (already available with the current version) or via an external /PHYReset at pin 8D (new version).

This modification has made the design of your customized Carrier Board simpler and more reliable. The new component no longer requires an additional 2.5 V on the Ethernet transformer, instead all that is needed is the primary 3.3 V supply voltage.

The Signal ETH\_NWAYEN now extends to pin 41C (10k pull-up).

(Located in the data sheet under: Ethernet-PHY LED3). Now there is an Ethernet status display available (e.g. Traffic-LED). For more details refer to the applicable Ethernet PHY data sheet.

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- 3. PCI:
  - 10 kOhm pullup resistor has been added to the /PCI-Reset line enabling a more reliable detection of any connected PCI devices (in the PCB revision 1245.0 under certain circumstances devices were recognized that were not connected).
- 4. Additional Module Connections:
  - Signal ETH TXD1 available at pin 8C (10 kOhm pull-up). This ٠ makes it possible to boot from various ranges (low=0x00000000) or high (= 0xFFF00000) within the Flash to suit a variety of uses. Default is Boot high; Boot low is possible by connecting 4.7 kOhm pull down. а
  - Signal Test\_Sel\_1 was added at pin 32B (10k PD) This allows universal use of the local Plus Bus
  - Signal ETH\_RXD1 (J1850\_RX) at pin 33B and ETH\_TXD3 (J1850\_TX) at pin 33A added. This allows use of the J1850 interface on phyCORE modules that are shipped without Ethernet PHY at U2 populated.

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