PHYTEC

TouchPanel-537

Hardware-Manual

Edition: January 1997

A product of a PHYTEC Technology Holding company

In this manual are descriptions for copyrighted products which are not explicitly indicated as such. The absence of the trademark (©) symbol does not infer that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual

The information in this document has been carefully checked and is believed to be entirely reliable. However, PHYTEC Meßtechnik GmbH assumes no responsibility for any inaccuracies. PHYTEC Meßtechnik GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product. PHYTEC Meßtechnik GmbH reserves the right to alter the information contained herein without prior notification and accepts no responsibility for any damages which might result.

Additionally, PHYTEC Meßtechnik GmbH offers no guarantee nor accepts any liability for damages arising from the improper usage or improper installation of the hardware or software. PHYTEC Meßtechnik GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 255 Ericksen Avenue NE Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	+1 (800) 278-9913 info@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	+1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	+1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

1st Edition: January 1997

Preface 1
1 Introduction 1
2 The first commissioning or Getting started 7
3 Possibilities for connecting external Peripheries 9
3.1 The strip connectors 9
3.2 The Signal- and Portconnectors 10
4 Jumper 13
4.1 Jumper groups 13
4.2 Placement of jumper 14
4.3 Setting of the jumper 15
4.3.1 The jumper setting for SERIAL1 15
4.3.2 Jumper settings for the A/D-Converter 16
4.3.3 Jumper setting Real-Time Clock 16
4.3.4 Jumper setting for contrast 16
4.3.5 Jumper setting for external Keyboard 17
4.3.6 Jumper setting of the address decoder 17
4.3.7 Jumper setting for memory equipment 17
4.3.8 Jumper settings for battery backup 18
4.3.9 Jumper setting for the Controller settings 18
4.3.10 Jumper setting for the buzzer 19
5 The Address decoder / Memory organisation 21
5.1 The Address decoder 21
5.1.1 Address decoder EP 386 21
5.1.2 Address decoder EP 419 26
5.2 The Power-On-Jump-Option 32
5.2.1 Function of the decoder during a power-on 32
5.2.2 Creating your Software applications for Power-On-Jump 33
6 The usage of the SAB80C537-Pins 35
7 The serial ports 37
7.1 SERIAL0 37
7.2 SERIAL1 38
7.2.1 Transmit modes of SERIAL1 38
7.2.2 Selecting the Transmitting mode for SERIAL1 39
7.2.3 SERIAL1 to CAN 41
8 The Chip-Enable-Signals 42
9 The A/D-converter of the SAB80C537 43
10 The Real-Time Clock (RTC) RTC-72423A 45
10.1 Accessing the RTC 45
10.2 Connecting the RTC to the Controller 46

11 The CAN-Controller 47
12 The LC-Display 48
12.1 Changing the Contrast 48
13 The LCD-Controller 49
13.1 Memory of the SED1330F 49
13.2 Addressing of LCD-Controller 50
14 The TouchPanel 51
15 External Keyboard 53
15.1 Supported keyboards 53
15.2 The characterset 53
15.3 The keyboardinterface 53
15.4 The Jumpers for the Keyboard-Interface 54
15.5 The Keyboard driver 54
16 The Buzzer 55
17 Memory configuration 57
17.1 Memory expansion 57
17.1.1 Default memory size 57
17.1.2 RAM-expansion with U9 58
17.1.3 Expansion on U11 58
18 The RAM-write protection and the battery backup 61
19 The RAM-Deselecting for the Power Down/Idle-Mode 63
20 The input ports of the Controller 64
20.1 Program execution from external/internal ROM 64
20.2 Power-Saving-Mode/Watchdog-Enable 64
20.3 Oscillator-Watchdog-Enable 64
21 The Banklatch U15 65
22 The RESET-Signal 67
23 Flash utilities 68
23.1 Starting the Flash utilities 68
23.2 Flash-programming 68
23.3 RAM-Download 69
24 Appendix 71
24.1 Troubleshooting 71
Index 73

Table of figures

Figure 1: Schematic....4
Figure 2: Component placement....4
Figure 3: Dimensions of the TouchPanel-537....6
Figure 4: Position of Connections, View of Placement....11
Figure 5: Placement of connectors, solderside view....11
Figure 6: Position of the connector groups in the padfield (top View)....12
Figure 7: Jumper positions, component side....14
Figure 8: Jumper positions, solder side....14
Figure 9: Pin assignment of the SUB-DB9-Connector X4, Front view....37
Figure 10: Pin assignment for RS-232, Front view....38
Figure 11: Pin assignment for a RS-285 Connection, Front view....38
Figure 12: Pin assignment according to CiA/DS102-1 spec., Front view ...38
Figure 13: Position of Jumpers necessary to change the desired transfer mode....39
Figure 14: Pin assignment of the external reference voltage input X8....43
Figure 15: Position of X8 and JP4,JP5....44
Figure 16: Positions of the Jumpers JP6....46
Figure 17: Position of adj. resistor RS1, adj. connector X11 and the Jumper JP15....48
Figure 18: The memory map of the LCD-Controller....49
Figure 19: Keyboard interface X12, viewed from the connectorside....53
Figure 20: Position of Jumpers for keyboard and connector X12....54
Figure 21: Position of the Jumper JP40....55
Figure 22: Position of the Jumper to configure the memory used....59
Figure 23: Battery connector X2....62

Preface

This TouchPanel-537 User's Manual describes the board's design and functions. Precise specifications for the C540U/C541U microcontrollers can be found in the enclosed microcontroller Data-Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding EMV-Conformity of the PHYTEC TouchPanel-537

PHYTEC miniCON Single Board Computers (henceforth „products") are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

PHYTEC products must be operated within protective, grounded circuitry. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the products' pin header rows are longer than 3 m.
Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, EMV-Statutes. Only after doing so the devices are allowed to be put into circulation.

PHYTEC products fulfill the norms of the EMVG-statute only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

It is necessary that only appropriately trained personnel (such as electricians) handle and/or operate these products. PHYTEC products lacking protective enclosures are furthermore subject to damage by ESD and, hence, may only be unpacked, handled, operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers.

The TouchPanel-537 is one of a series of PHYTEC miniCONs which can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common Infineon's 8- and 16-bit controllers in two ways:

(1) as the basis for Starter Kits in which user-designed hardware can be implemented on a wrap-field around the controller and

(2) as universal, insert-ready, fully functional micro- and mini-MODULS which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. Please contact PHYTEC for additional information:

	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 255 Ericksen Avenue NE Bainbridge Island, WA 98110 USA
Web Site:	http://www.phytec.de	http://www.phytec.com
e-mail:	info@phytec.de	info@phytec.com
Voice:	+49 (6131) 9221-0	+1 (800) 278-9913
Fax:	+49 (6131) 9221-33	+1 (206) 780-9135

1 Introduction

The TouchPanel-537 from the PHYTEC Company provides a microcontroller board which serves excellent as a Man-Machine-interface for a wide variety of Applications.

The Combination of a programmable Controller and a graphic capable LCD allow a inexpensive way to provide a up-to-date menu-based user interface allowing communication to the Application. The supplied software tools for handling the Display and the TouchPanel are easily accessed through your C- or assembler program. The Display itself provides next to a textlayer a graphiclayer. When displaying the are both overlaid, enabling a neat and simultaneous display of Text and Graphic.

The wide variety of supplied Interfaces of the TouchPanel-537 allow a connection to existing or new developments with a very little effort. Especially worth mentioning is the network interface. This allows the Module to be used as a full CAN-Networkstation, controlling or as example handling other CAN-Stations of a widely spread network. The sampled input data or pre-sets can then be distributed to each subsystem individual. To centralize the via CAN-Net available information's and to Visualize the data could be one of the many applications.

Next to the widespread CAN-Bus the TouchPanel-537 can also be used in a RS-285-Network. The PHYTEC specific µNET is a good example for this area of application.

As a conception the TouchPanel-537 can be used as a additional self-sufficient user-interface in a existing application. Through the above mentioned network interfaces the data incurred in a existing system can be handled with a minimum increase load of the involves components.

Additionally to using the TouchPanel-537 as a pure mini-terminal, the controller could be unable for taking over measure and regulating-tasks. For this use of application the TouchPanel-537 is equipped with efficient components like Timers/Counters and A/D-converters.

As an interface to the ambient, the remaining I/O pins of the 80C537 can be used individually. Alternative to the TouchPanel-537 solution, a custom PCB with additional or modified I/O-Interface is possible, enhancing the field of application.

Enabling a fast and efficient way of creating even most complex Applications for the TouchPanel-537, we supply you an extensive software library. This library contains a wide range of functions to display Text and Graphics, but also the handle the TLC and/or an connected PC-Keyboard. The functions provide a C- and assembler interface to the proven to be worthwhile 8051-development software from the Keil Electronic company.

The TouchPanel-537 provides the following Features:

- Systemboard placed on a standardized 160 x 100 mm PCB
- Controller SAB80C537 or SAB80C517A
- LCD-Display (Display area 96 mm x 72 mm, Resolution 320 x 240 Pixel) with backplane illumination (Cold-Cathode Lamp)
- TouchPanel with 10 x 6 Keys (Keypad size 9 x 11 mm)
- Connector for a external PC-Keyboard
- single power supply 5 V ± 5 %, 700 mA regulated
- Improved fault-proof design through multilayer technology
- optional 128 kB Flash on-board (DIL)[1]
- on-board flash-programming
- No separate programming voltage required during Flash programming due to 5 V programmable Flash-memories
- 64 kB RAM on-board (optional up to 160 kB)[1]
- Additional up to 32 kB E(E)PROM[1]
- Battery backed memory and Real-Time Clock optional
- All port-, data- and address signals are assessable on the centered PCB-rap-field
- Bank latches for Flash and RAM are integrated in the address decoder
- RS-232 Interface with a SUB-DB9-Connector named X4
- Additional SUB-DB9-Connector, alternatively RS-232, RS-485 or CAN (BASIC-CAN)
- CAN- Interface optically coupled
- 5 available Chip Select signals for easy connection to external Peripheries
- Real-Time Clock
- Buzzer

[1] : other options can be found in the distributer catalog of PHYTEC

Schematics

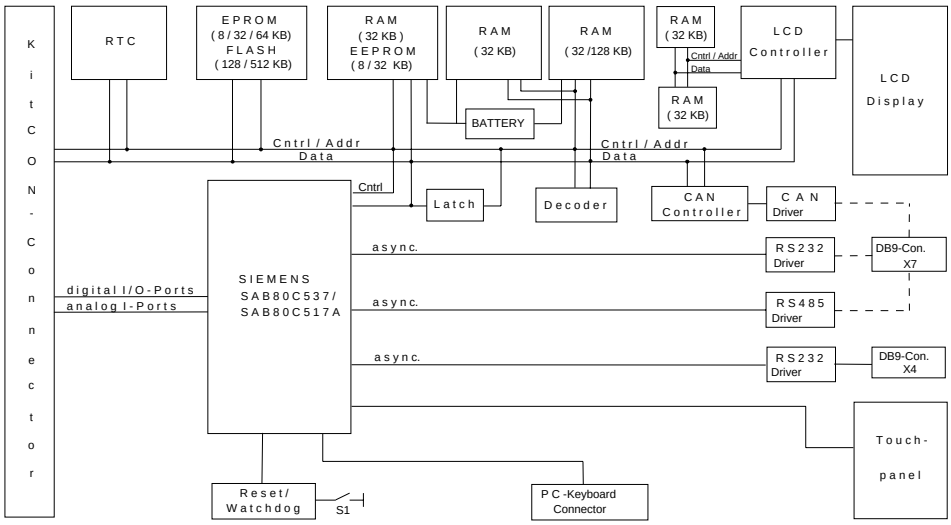


Figure 1: Schematic

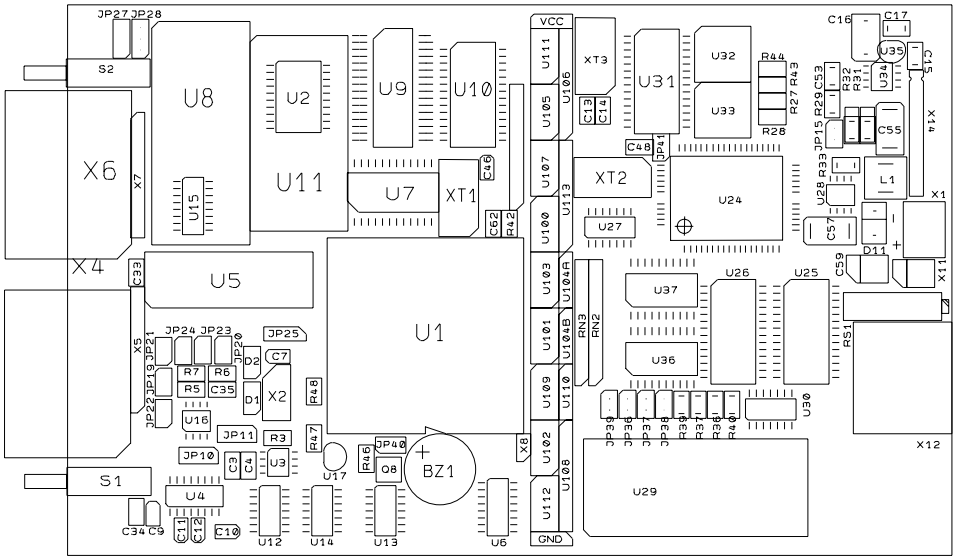


Figure 2: Component placement

Module hardware description general

The TouchPanel-537 is usually only delivered together with the LC-Display. Because of that the module consists of the controller board and the LCD-PCB. Both are connected electrically and mechanically. These are the universal SAB80C537-based TouchPanel-537 including the LCD-Controller- and the LC-Display including the Touch-Key-panel. Both modules have the mentioned size of 100 x 160 mm. The effective height due to the sandwich technology adds up to approximately 5 cm. The entire XY-size adds up to 169 x 100 mm because of the on-board-connectors (RS-232 etc.).

The TouchPanel-537 has two SUB-DB9 Connectors on the left size for the serial port and the CAN-Bus. On the right-hand side is a standard 5 Pin PC/XT/AT-Keyboard connector. Also on the right-hand side is a double screw connector for the voltage supply. The LCD-Illumination is also connected through one connector on the right-hand side. Two additional connectors, the LCD and the TouchPanel, are connected to the backside of the Controller-PCB. A optional available external contrast regulation can be connected to the Unit; otherwise the on-board contrast regulator can be used being right next to the keyboard connector

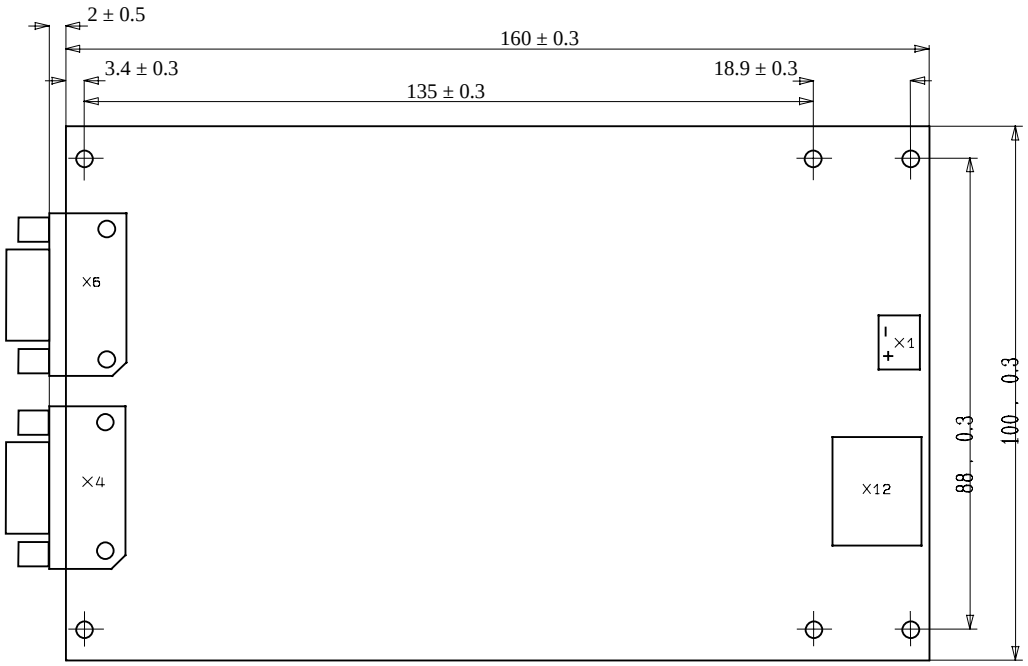


Figure 3: Dimensions of the TouchPanel-537

Power supply

The TouchPanel-537 requires only a single power supply providing a regulated voltage of 5 V ± 5 %. The backplane illumination is also supplied by the 5 V however being converted on-board to the special requirements of the LCD-lamp. Depending on the duty and options chosen on the TouchPanel-537 the peak current accumulates to a maximum of approx. 700 mA.

For backing up the on-board RAM and Real-Time Clock a low capacity battery can be used (100 mAh).

2 The first commissioning or Getting started

On the following pages you will find some hints to enable the first commissioning. We recommend that the monitor software from Keil Electronic is used. The monitor can be purchased in a EPROM or as a custom modifiable Software package from the Vendor of the TouchPanel-537. All hints in the following presume the use of the up-to-date Keil-monitor or a newer Version of the monitor.

- First of all you need a TouchPanel-537 with the specific EPROM installed in socket U8, containing the mentioned monitor program and a IBM-compatible PC.
- Connect one of the serial ports of your PC with the SUB-DB9 socket of the TouchPanel-537. The pins must be connected as follows:

  Pin 2: TxD of TouchPanel-537
  Pin 3: RxD of TouchPanel-537
  Pin 5: Signalground
- You do not require any further hand shake signals. The handshake is handled by the monitor software.
- Check that jumper JP25 is in position 2 - 3.
- Apply the supply voltage to the TouchPanel-537. Connect a 5 V power supply to the TouchPanel-537 connector X1. The power supply must provide at least 700 mA if required.
- Invoke the Terminal program MON51.EXE on your Host-PC by entering *mon51* for COM1: and *mon51 2* for COM2.
- Other communication or terminal programs are not suitable for data transmission to and from the Monitor on the TouchPanel-537, as a special transmission protocol is required. Ensure that only DOS is active at the time of the invocation.
- Push the Reset on the TouchPanel-537.

- After a successful start the sign-on will appear with a '#' as prompt. Now you load your own programs or a sample program by starting the 'load'-command. See on-line help for more details.
- If you should have problems during your transfer, the serial connection can easily be checked by shorting the RxD- and TxD-pins of the serial cable. Pressing any key of the PC will be echoed directly by the terminal program after it has displayed '*** Terminal Mode ***'.

If you are using a EPROM-simulator or a EPROM we recommend the Memory configured as MODE0 (JP25 on 1 - 2).

If problems are still occurring refer to the addendum of the handbooks before calling the Hotline.

3 Possibilities for connecting external Peripheries

3.1 The strip connectors

The TouchPanel-537 has the following Connectors available:

X1: Double screw connector for the power supply

X2: Triple pin connector for a backup battery providing power for the RAM and the Real-Time Clock

X4: SUB-DB9-Connector for RS-232-Signal of the first serial connector

X5: 9 Solder pads with all signals of the X4 connector available

X6: SUB-DB9-Connector for RS-232-signal or the RS-485-signal of the second serial port of the Controller or the optical coupled CAN-businterface

X7: 9 Solder pads with all signals of the X6 connector available

X8: 2 Solder pads to connect a optional external reference voltage needed for the A/D-converter of the SAB80C517

X9: 20-pin Socket to connect the TouchPanel

X10: 3-pin Plug to connect the backplane illumination from the LCD to the on-board-supply. Mind your fingers! **(HIGH VOLTAGE: up to 1kV AC !)**

X11: 3 Solder pads for a external contrast regulator

X12: 5-pin Socket for connecting a PC/XT/AT-Keyboard

X13: 14-pin socket for the LC-Display

X14: 9-Solder pads with all signals of the CAN-businterface for a connection alternative to the connection via the SUB-DB9-Socket X6

3.2 The Signal- and Portconnectors

The TouchPanel-537 provides all control- and portpins via a solder pad area placed near the center of the systemboard. These pads can be connected with a suitable socket or similar to any hardware improving and/or expanding the capabilities of the entire system to your needs.

The signals of the solder pad area are separated into functional groups which are named U100 to U113. The exact placement is shown in the following diagrams.

The following Signals group together:

U100:	P1.0 .. P1.7	(P1.0 ->Pin 1 of U100)
U101:	P3.0 .. P3.7	(P3.0 ->Pin 1 of U101)
U102:	P4.0 .. P4.7	(P4.0 ->Pin 1 of U102)
U103:	P5.0 .. P5.7	(P5.0 ->Pin 1 of U103)
U104:	P6.0 .. P6.7	(P6.0 ->Pin 1 of U104A)
U105:	Databus	(D0 -> Pin 1 from U105)
U106:	Addressbus low	(A0 -> Pin 1 from U106)
U107:	Controlbus	FL_PRG (Pin 4), BNK (Pin 5), /HWPD (Pin 7), B2 (Pin 8)
U108:	Reset signal	RES2, /RES, /RO,RES, B-RES & Chip-Select signal /EW5, /EW8 (RES2 -> Pin 1, all others serially numbered)
U109:	P7.0 .. P7.7	(P7.0 ->Pin 1 of U109)
U110:	P8.0 .. P8.3	(P8.0 ->Pin 1 of U110)
U111:	Addressbus high	(A8 -> Pin 1 of U111)
U112:	Chip-Select signal	/EW1../EW4, /EW6, /EW7 (/EW1 -> Pin 1, all others serially numbered)
U113:	Controller-Signals	ALE (Pin 1), PSEN (Pin 2), PWR (Pin 4), /WR (Pin 5), /RD (Pin 6)

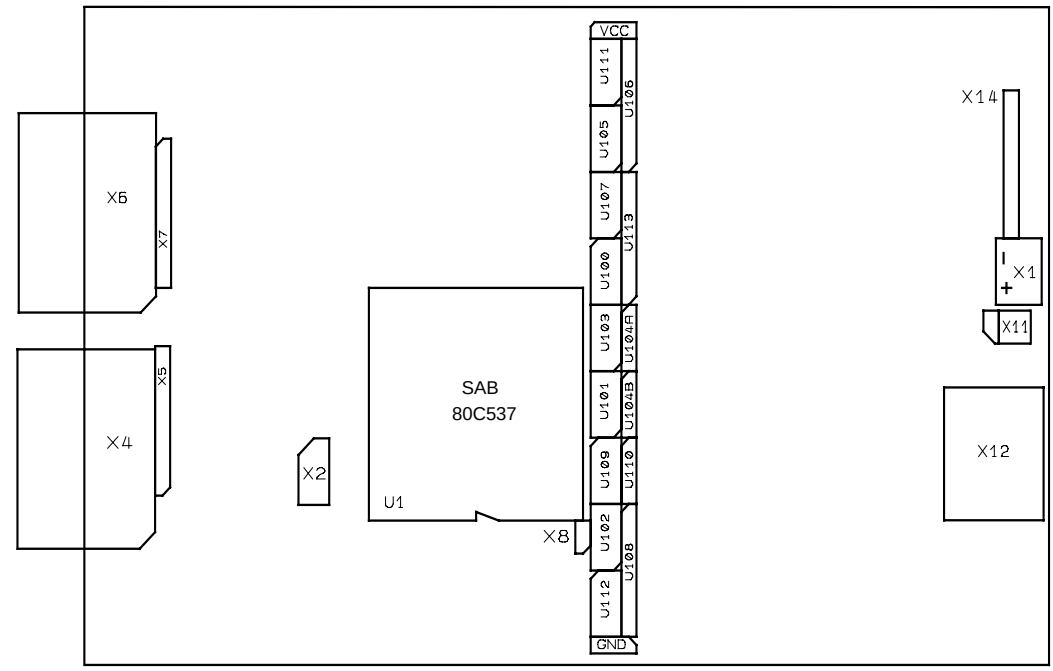


Figure 4: Position of Connections, View of Placement

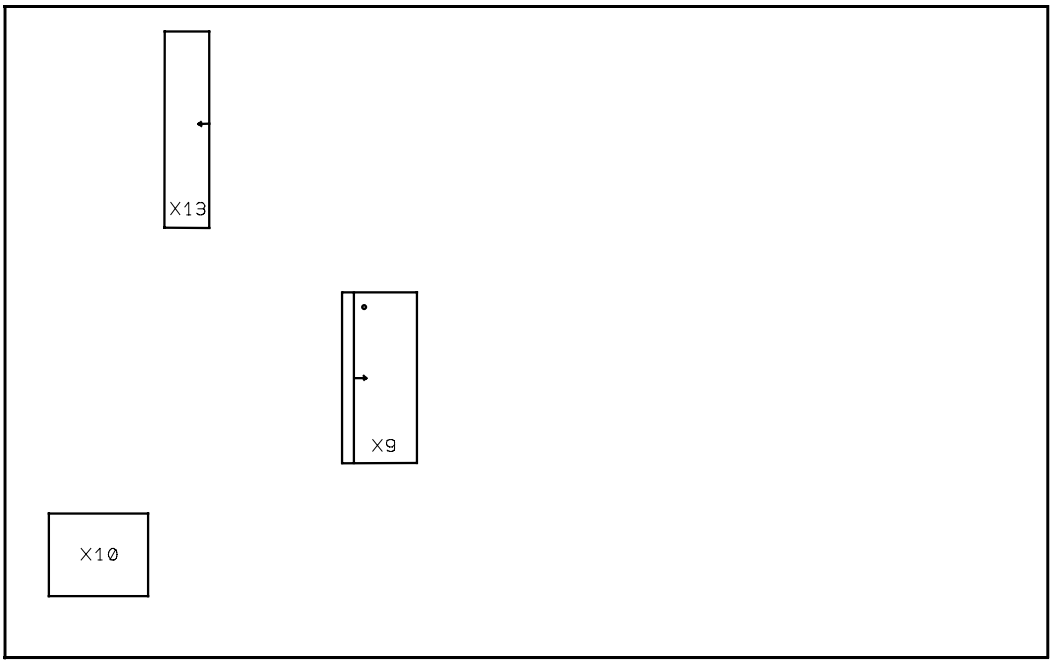
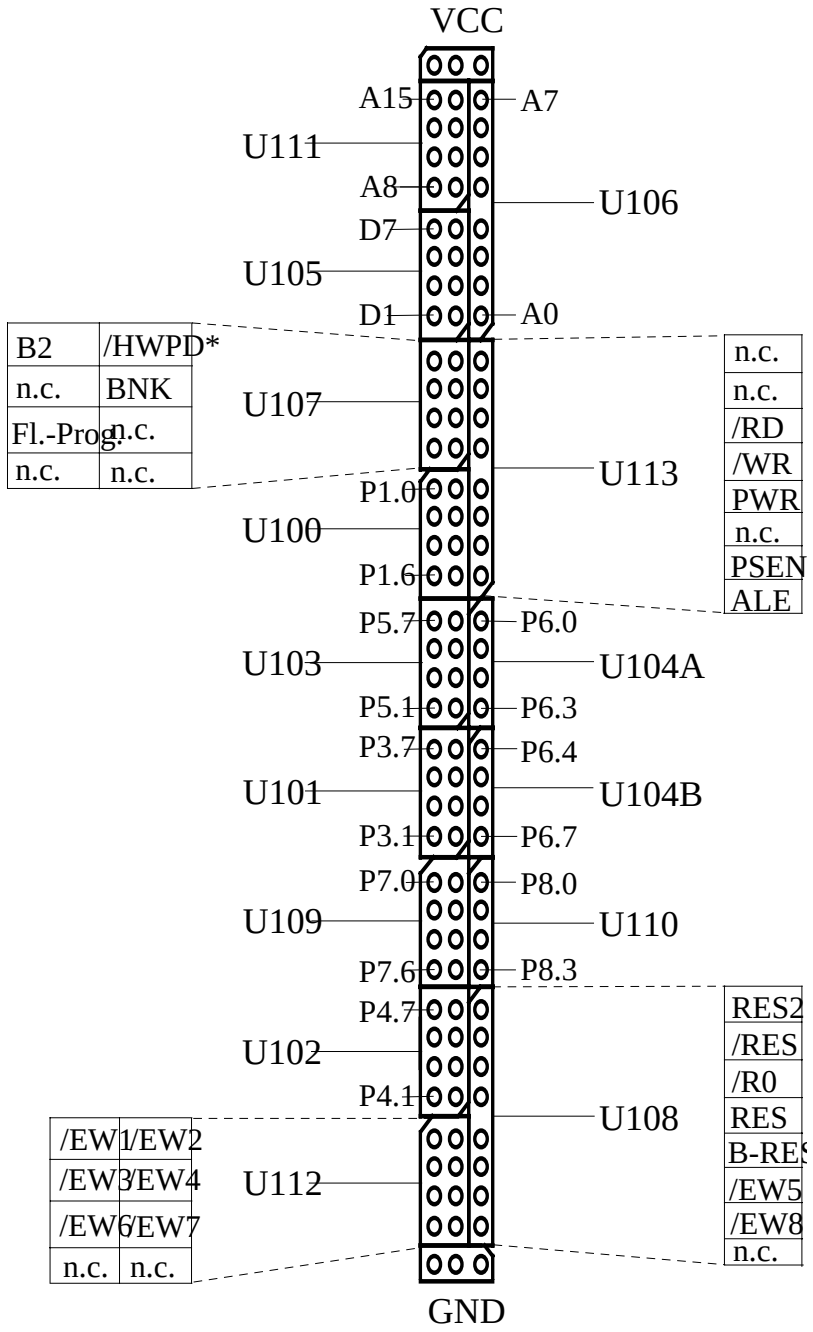


Figure 5: Placement of connectors, solderside view



* only 80C517A, otherwise GND via JP33

Figure 6: Position of the connector groups in the padfield (top View)

4 Jumper

To set-up the basic functions of the TouchPanel-537 only few jumpers have to be set. The dominant amount of Jumpers is only used to support very special applications.

The few main jumpers are set by factory default. This usually makes changes unnecessary.

4.1 Jumper groups

The following list of jumpers are grouped to function groups. A precise description of the setting is found in the related section.

JP1..JP3:	Controller jumper
JP4,.JP5:	Analogue reference voltage;
JP6:	Real-Time Clock, CAN-Controller
JP10, JP11, JP16, JP17:	Driver for SERIAL1
JP12, JP13, JP19..JP24, JP34:	Connection of SUB-DB9-connector X6
JP14:	Bootstrap-Mode
JP15:	Contrast
JP25:	Modeselector for the address decoding
JP26:	Generating the /CE-extension
JP27, JP28:	EPROM-/Flash selection U8
JP29..JP32:	memory selection U11
JP33:	Hardware-Power-Down (only 80C517A)
JP36..JP39:	Keyboard interface
JP40:	Enable/Disable buzzer
JP41:	CAN-Controller

4.2 Placement of jumper

The following picture helps you find jumpers on the TouchPanel-537.

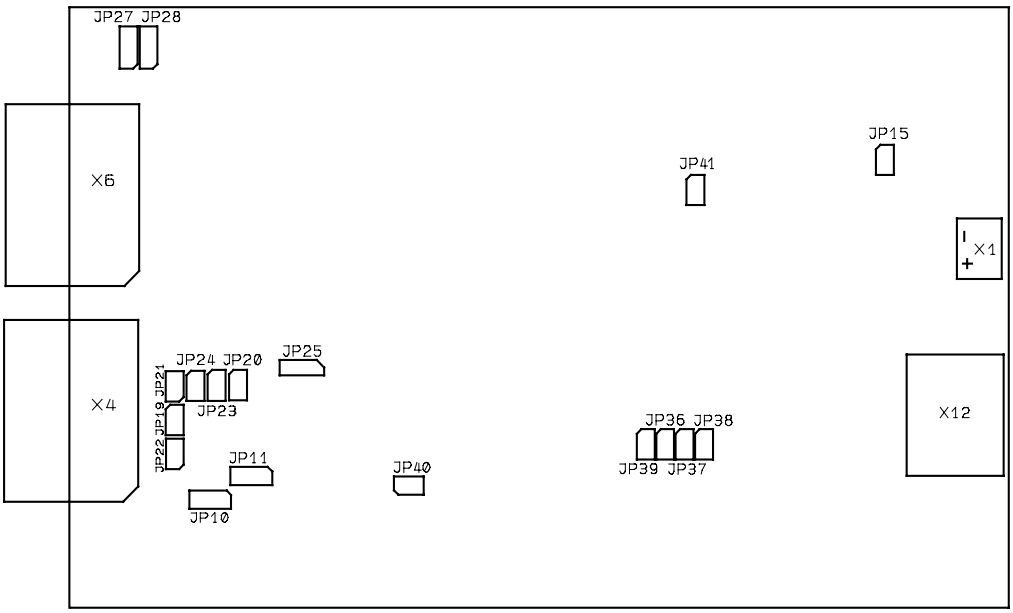


Figure 7: Jumper positions, component side

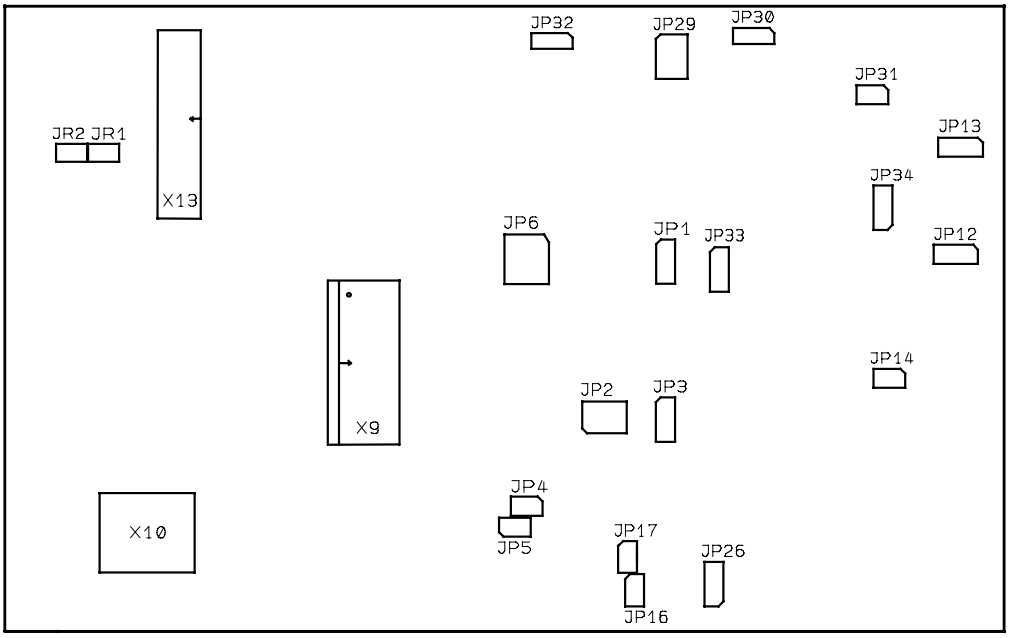


Figure 8: Jumper positions, solder side

4.3 Setting of the jumper

4.3.1 The jumper setting for SERIAL1

SERIAL1 (X6) nach	**RS-232**	**RS-485**	**CAN**
JP6	don't care	don't care	7 - 8/8 - 9[1]
JP10, 11	1 - 2	2 - 3	don't care
JP12, 13	1 - 2	open	2 – 3
JP16	open	for µNet[2]	don't care
JP17	open	don't care[3]	don't care
JP19, 20, 21, 22	open	don't care[4]	open
JP23, 24	open	closed	open
JP34	open	1 - 2/open[5]	2 - 3
JP41	don't care	don't care	closed

[1]: **Attention!** JP6 selects INT0 or INT1 for the CAN-Controller. INT0 can also be used for SERIAL1 (RS-285). If INT0 is used for the CAN-Controller JP16 must be open. Because the RTC may be connected via JP6 to INT0 or INT1 you must take precaution not to cause any conflicts.

[2]: To connect RxD to the bit-addressable Port 3.2 JP16 must be closed. **Warning!** JP6 can also be used to connect STD.P from the RTC or /INT of the CAN-Controller to Port3.2. Therefor you must make sure that if using µ-NET JP6 may not be on position 5 - 6 nor 8 - 9.

[3]: The transmitter of the RS-285-device is disabled by factory default with Pull-Up R9. By closing Jumpers 17 the control of the send function can be controlled with Port 1.1.

[4]: By closing jumper JP19, JP20, JP21 and JP22 the resistors R5,R6,R7, if available on the PCB, can be used to connect a RS-285-network.

[5]: The supply voltage can be accessed from the SUB-DB9-connector X6 by closing Jumper JP22 and Jumper JP34 must be on position 1 - 2. Otherwise JP34 has to be open.

4.3.2 Jumper settings for the A/D-Converter

Function	**JP4**	**JP5**
External reference voltage	open	open
VCC and GND as reference	closed	closed
voltage		

4.3.3 Jumper setting Real-Time Clock

Function	**JP6**
Clksource for Timer 0 from RTC	1 - 2
Clksource for Timer 1 from RTC	2 - 3
Interrupt /INT0 from RTC Clocksignal	5 - 6[1+2]
Interrupt /INT1 from RTC Clocksignal	5 - 4[1+2]

4.3.4 Jumper setting for contrast

Function	**JP15**
manual contrast setting via adj. resistor	open
software controlled contrast	closed
via Portpin 1.2	

[1] : **Attention!** INT0 may be used for SERIAL1 to RS-485. If using INT0 for the RTC jumper JP16 must be opened.

[2] : **Attention!** INT0 may be used for SERIAL1 to RS-485. If using INT0 for the RTC jumper JP16 must be opened.

4.3.5 Jumper setting for external Keyboard

Function	**JP36 - JP39**
no external Keyboard connected	open
external Keyboard connected	closed

4.3.6 Jumper setting of the address decoder

Function	**JP25**
Memorymap MODE0	1 - 2
Memorymap MODE1	2 - 3

4.3.7 Jumper setting for memory equipment

EPROM on U8:	**JP27**	**JP28**
8 kB EPROM	1 - 2	1 - 2
32 kB EPROM	1 - 2	2 - 3
64 kB EPROM	2 - 3	2 - 3
128 kB Flash	2 - 3	2 - 3

EEPROM/EPROM / RAM on U11	**JP29**	**JP30**	**JP31**	**JP32**
8 kB EEPROM	2 - 3	2 - 3	open	1 - 2
32 kB EEPROM	2 - 3	1 - 2	open	1 - 2
32 kB RAM	2 - 3	1 - 2	open	2 - 3
8 kB EPROM	1 - 2	2 - 3	1 - 2	1 - 2
32 kB EPROM	2 - 5	2 - 3	1 - 2	1-2

4.3.8 Jumper settings for battery backup

Supply of U11	**JP32**
VPD	2 - 3 ; RAM only
VCC	1 - 2 ; EPROM and EEPROM

If you forget to place JP 32 correct, a fast discharged battery will be the consequence if a EPROM or EEPROM in U11 is used instead of a RAM.

4.3.9 Jumper setting for the Controller settings

Selecting the program origin

Function (Code memory access)	**JP1**
below 2000h internal access, from 2000h ex-ernal	2 - 3
from 0000h to FFFFh only external	1 - 2
ROM-les Version (80C537 etc.)	1 - 2

Power-Saving-Mode/Watchdog-Enable

Function	**JP2**
PD, IDLE and SLOW-Mode enable/	2 - 4
Watchdog disable	
PD, IDLE and SLOW-Mode enable	2 - 1
PD, IDLE and SLOW-Mode disable/	2 - 5
Watchdog start	
PD, IDLE and SLOW-Mode disable	2 - 3

Oscillator-Watchdog-enable

Function of the Oscillator-WD	**JP3**
Watchdog on	2 - 3
Watchdog off	1 - 2

4.3.10 Jumper setting for the buzzer

Function	**JP40**
Buzzer disabled	open
Buzzer via Port P6.0	closed

controlled

5 The Address decoder / Memory organisation

5.1 The Address decoder

The address recognition is handled by a EPLD 5c060, EP600 or GAL20V8. Due to improvement and enhancement of our product, we reserve the right to change the logic device or the Programming of the devices.
The shown programming procedures in this chapter are only valid with the explicit named decoder labels.

We also provide inexpensive custom decoders on your request. This enables you to have a (as long as technical possible) custom specific Memory- and IO-map meeting your needs.

5.1.1 Address decoder EP 386

The EP 386 represents the standard decoder. It supports 32 k EPROM's as well as the MODE0 memory layout which equals the Harvard architecture. Also supported is the MODE1 memory layout, a von-Neumann architecture (see following memorymap).

The Gal-sourcelisting

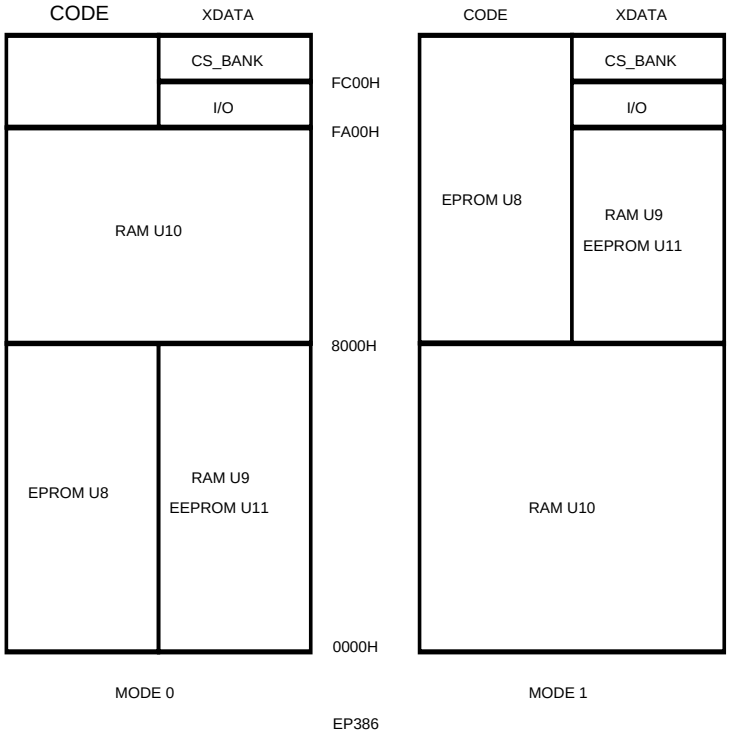
```
*IDENTIFICATION
 EP386 Adreßdecoderpal für miniCON537/TLC mit EPLD 5C060.
 PHYTEC , 15.8.95 bh

*PAL
 TYPE = 5C060

*DECLARATIONS
 X-VAR = 12;
 Y-VAR = 9;

*X-NAMES
 PSEN,RD,RES,MODE,BNK,A15,A[11..9],SWITCH,FLPRG,IO;

*Y-NAMES
 CSROM,CSRAM1,CSRAM2,CSEE,RRD,CSBANK,EW,SWITCH,OEROM;

*RUN-CONTROL
 CPU-TIME = 100;
 PROGFORMAT = JEDEC;
 LISTING = EQUATIONS;

*BOOLEAN-EQUATIONS
 SWITCH := A15 + SWITCH ;Aktivierung der Decodierung bei Zugriff
                  ,auf 8000H


*FUNCTION-TABLE
$ A15 ,(A[11..9]) , IO  , RD  , PSEN      ,MODE , BNK , SWITCH    ,
RES   ,FLPRG      : CSROM     ;                                  U8
     0      ,  0H..7H   ,  -         ,  -         ,      0    ,
0     ,  -         ,     -     ,   1       ,     -     :     0     ;
00H-7FH     ,                                                  PSEN
      -     ,  0H..7H   ,  -         ,  -         ,      0    ,     1
      ,  -         ,     0     ,   1       ,     -     :     0     ;
00H-FFH     ,                                                  PSEN
     1      ,  0H..7H   ,  -         ,  -         ,      0    ,     1
      ,  -         ,     1     ,   1       ,     -     :     0     ;
80H-FFH     ,                                                  PSEN
REST
                        :     1     ;

$A15  ,(A[11..9]) , IO  , RD  , PSEN      ,MODE , BNK , SWITCH    ,
RES   ,FLPRG      : OEROM     ;  U8
     -      ,  0H..7H   ,  -         ,  -         ,     0     ,     -
      ,  -         ,     -     ,   -       ,     -     :     0     ;
PSEN
REST
                        :     1     ;
```



```
$ A15 ,(A[11..9]) , IO  , RD  , PSEN      ,MODE , BNK , SWITCH    ,
RES   ,FLPRG      :CSRAM1     ; U9 aux RAM
     0       ,  0H..7H   ,  -         ,  -         ,      1      ,      0
       ,  1         ,      -      ,    1       ,      -      :      0      ;
00H-7FH     ,                                                            RD
     1       ,  0H..7H   ,  0         ,  -         ,      1      ,      1
       ,  1         ,      -      ,    1       ,      -      :      0      ;
80H-EFH     ,                                                            RD
     1       ,  0H..4H   ,  1         ,  -         ,      1      ,      1
       ,  1         ,      -      ,    1       ,      -      :      0      ;
F0H-F9H     ,                                                            RD
REST
                         :     1     ;


$ A15 ,(A[11..9]) , IO  , RD  , PSEN      ,MODE , BNK , SWITCH    ,
RES   ,FLPRG      :CSRAM2     ;          U10          std          RAM
    1        ,  0H..7H   ,  0   ,  -  ,      -      ,      0      ,  -
       ,      -      ,    1       ,      -      :      0      ; 80H-EFH   ,
VN
    1        ,  0H..4H   ,  1   ,  -         ,      -      ,      0      ,
-      ,      -      ,    1       ,      -      :      0      ; F0H-F9H   ,
VN
    0        ,  0H..7H   ,  -   ,  -         ,      1      ,      1      ,
-      ,      0      ,    1       ,      -      :      0      ; 00H-7FH   ,
VN
    0        ,  0H..7H   ,  -         ,  -         ,      -      ,      1
       ,  -         ,      1      ,    1       ,      -      :      0      ;
00H-7FH     ,                                                            VN
REST
                         :     1     ;


$ A15 ,(A[11..9]) , IO  , RD  ,PSEN ,MODE ,BNK  ,SWITCH     ,RES
      ,FLPRG      :     CSEE  ; U11 EEPROM/RAM
    0        ,  0H..7H   ,  -         ,  -         ,      1      ,      0
       ,  0         ,      -      ,    1       ,      -      :      0      ;
00H-7FH     ,                                                            RD
    1        ,  0H..7H   ,  0         ,  -         ,      1      ,      1
       ,  0         ,      -      ,    1       ,      -      :      0      ;
80H-EFH     ,                                                            RD
    1        ,  0H..4H   ,  1         ,  -         ,      1      ,      1
       ,  0         ,      -      ,    1       ,      -      :      0      ;
F0H-F9H     ,                                                            RD
REST
                         :     1     ;


$ A15 ,(A[11..9]) , IO  , RD  ,PSEN ,MODE ,BNK  ,SWITCH     ,RES
      ,FLPRG      :     RRD   ;
    0        ,  0H..7H   ,  -   ,  0  ,      -      ,      0      ,  -
       ,      -      ,    1       ,      -      :      0      ; RAM    00H-
7FH
    1        ,  0H..7H   ,  0         ,  0         ,      -      ,      0
       ,  -         ,      -      ,    1       ,      -      :      0      ;
EEPROM                                                                  80H-EFH
    1        ,  0H..4H   ,  1         ,  0         ,      -      ,      0
       ,  -         ,      -      ,    1       ,      -      :      0      ;
EEPROM                                                                  F0H-F9H
    1        ,  0H..7H   ,  0         ,  -         ,      0      ,      0
       ,  -         ,      -      ,    1       ,      -      :      0      ;
EEPROM 80H-EFH
```

```
    1       ,  0H..4H   ,  1        ,  -        ,     0     ,     0
      ,  -        ,     -     ,   1       ,     -     :     0     ;
EEPROM                                                        F0H-F9H
    0       ,  0H..7H   ,  -        ,  0        ,     -     ,     1
      ,  -        ,     -     ,   1       ,     -     :     0     ;
RAM                                                           00H-7FH
    0       ,  0H..7H   ,  -        ,  -        ,     0     ,     1
      ,  -        ,     1     ,   1       ,     -     :     0     ;
RAM                                                           00H-7FH
    1       ,  0H..7H   ,  0        ,  0        ,     -     ,     1
      ,  -        ,     -     ,   1       ,     -     :     0     ;
RAM                                                           80H-EFH
    1       ,  0H..4H   ,  1        ,  0        ,     -     ,     1
      ,  -        ,     -     ,   1       ,     -     :     0     ;
RAM                                                           F0H-F9H
REST
                        :     1     ;


 $ A15   ,(A[11..9]), IO, RD   ,PSEN  ,MODE,BNK ,SWITCH,RES   ,FLPRG
      :   EW ;
     1   ,      5H  ,  1    ,  -   ,   1   , -   ,  -   ,      - ,
 1    ,   -  :  0  ; FA00H-FBFFH
 REST                                              :  1   ;

 $ A15   ,(A[11..9]), IO, RD   ,PSEN  ,MODE,BNK ,SWITCH,RES   ,FLPRG
      :CSBANK   ;
     1   ,  6H    ,  1  ,  -    ,  1   ,   -,  -    ,   -      ,   1
      ,   -  :  1  ; FC00H-FDFFH
 REST                                              :  0   ;

*PINS
 A[8]=1,A[9]=8,A[10]=7,A[11]=6,A[15]=2,
 CSROM=15,CSRAM1=16,CSRAM2=17,CSEE=18,OEROM=3,
 IO=4,FLPRG=5,RES=10,GND=12,MODE=14,SWITCH=21,RD=11,
 BNK=23,PSEN=9,EW=22,CSBANK=20,RRD=19,VCC=24;

*Special Functions
 SWITCH.CLK=/PSEN  ;
 SWITCH.RS =/RES ;

*Fuses
 $6406=BLOWN ;  Enable Clock-Option für Pin 21

*END
```

The memory layout



The I/O-area splits up as follows:

/CSRTC	FA00H..FA3FH (RTC)
/EW2	FA40H..FA7FH (CAN)
/EW3	FA80H..FABFH (LCD)
/EW4	FAC0H..FAFFH
/EW5	FB00H..FB3FH
/EW6	FB40H..FB7FH
/EW7	FB80H..FBBFH
/EW8	FBC0H..FBFFH

5.1.2 Address decoder EP 419

The address decoder EP 419 is a special version designed for the on board Flash programming. It supports 64 k EPROM's or 128 k Flash-Memories.
MODE0 is designed for programming Flash-Memory as well as executing the downloaded program from the Flash-Memory. On the other hand MODE1 is designed to download a program into and execute it from RAM.

The Gal-Source listing

```
*IDENTIFICATION
 EP466 Adreßdecoderpal für miniCON537/TLC FLASH-Version mit EPLD
 5C060.
 ersetzt P419
 PHYTEC , 28.5.97 be

*PAL
 TYPE = 5C060

*DECLARATIONS
 X-VAR = 14;
 Y-VAR = 8;

*X-NAMES
 PSEN,RD,RES,MODE,EW,CSBANK,BNK,A15,A[11..9],SWITCH,FLPRG,IO;

*Y-NAMES
 CSROM,CSRAM1,CSRAM2,CSEE,RRD,CSBANK,EW,OEROM;

*RUN-CONTROL
 CPU-TIME = 100;
 PROGFORMAT = JEDEC;
 LISTING = EQUATIONS;

*BOOLEAN-EQUATIONS
```



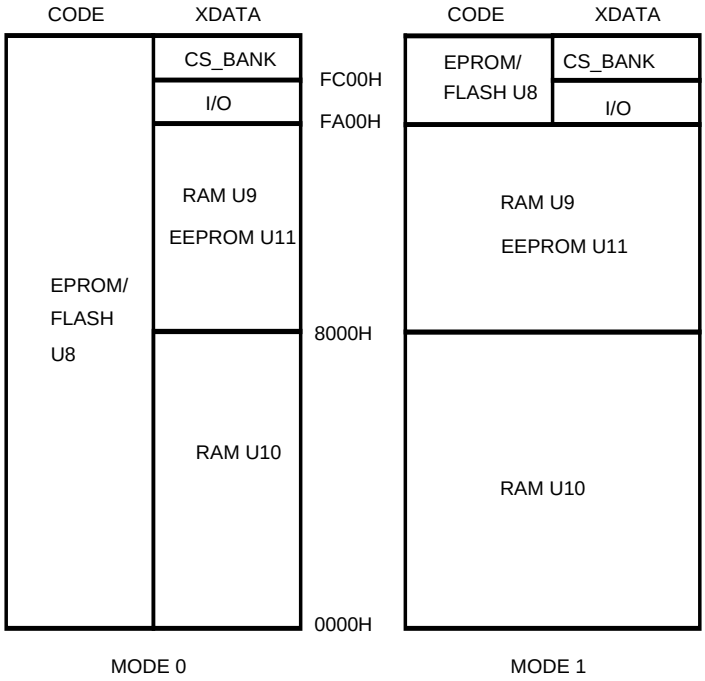
```
*FUNCTION-TABLE
$ A15 , (A[11..9])      , IO  , RD  , PSEN      ,MODE , BNK ,CSBANK
      ,EW   , RES ,FLPRG      : CSROM     ;   U8          CS   FLASH
      -     ,  0H..7H   ,  -  ,  -        ,     0     ,     -     ,
-     ,     -     ,     -     ,     1     ,     0     :     0     ;
00H-FFH,                                                      PSEN

      -     ,  0H..7H   ,  -  ,  -        ,     1     ,     0     ,
-     ,     0     ,     -     ,     1     ,     1     :     0     ;
00H-FFH-CSBANK,
RD/WR
      1     ,  5H..7H   ,  1  ,  -        ,     0     ,     1     ,
-     ,     -     ,     -     ,     1     ,     1     :     0     ;
FAH-FFH     ,                                                 PSEN
REST
                                      :     1     ;
$ A15                                                         ,
(A[11..9])                                                    , IO     ,
RD                                                            , PSEN
                                                              ,MODE    ,
BNK                                                           ,CSBANK
                                                              ,EW , RES
                                                              ,FLPRG   :
OEROM                                                         ;  U8    OE
FLASH
                                                              -,   0H..7H
                                                              ,   -   ,   -
                                                              ,   0     ,
                                                              -,   -     ,
                                                              -,  -      ,
                                                              -,  0      :
                                                              0;  00H-FFH
,                                                                    PSEN
                                                              -,   0H..7H
                                                              ,   -   ,   0
                                                              ,-  ,      0
                                                              ,   -      ,
                                                              0,  -      ,
                                                              -,  1      :
                                                              0;     00H-
FFH-
CSBANK,                                                             RD/WR
                                                              1   ,
5H..7H                                                        ,   1   ,   -
                                                              ,   0     ,
                                                              1   ,   -
                                                              ,   -     ,
                                                              -   ,     -
                                                              ,   1     :
                                                              0   ;  FAH-
FFH                                 ,                               PSEN
REST




                                                                 :     1
                                                              ;

$ A15                                                          ,
(A[11..9])                                                     , IO     ,
RD                                                             , PSEN
```

```
                                                    ,MODE   ,
BNK                                                 ,CSBANK
                                                    ,EW     ,
RES                                                 ,FLPRG
                                                    :CSRAM1;
U9                                aux                     RAM
                                                    1 ,
0H..7H                                              ,   -   ,
-                                                   , 1     ,
                                                    - ,  1
                                                    , 0     ,
                                                    1 ,     1
                                                    , 0     :
                                                    0 ;  80H-
F9H,                                                  RD/WR
                                                    1 ,
0H..7H                                              ,   -   ,
-                                                   , 0     ,
                                                    0 ,  -
                                                    , -     ,
                                                    - ,     1
                                                    , 1     :
                                                    0 ;  80H-
FFH,                                                  PSEN
                                                    1 ,
0H..7H                                              ,   -   ,
-                                                   , -     ,
                                                    1 ,  1
                                                    , 0     ,
                                                    1 ,     1
                                                    , 1     :
                                                    0 ;  80H-
F9H                                 ,                   VN
REST


                                                      :     1
                                                    ;

                                                    ,
$ A15                                               , IO    ,
(A[11..9])                                          , PSEN
RD                                                  ,MODE   ,
BNK                                                 ,CSBANK
                                                    ,EW     ,
RES                                                 ,FLPRG
                                                    :CSRAM2;
U10                               std                     RAM
                                                    0 ,
0H..7H                                              ,   -   ,
-                                                   , 1     ,
                                                    - ,  -
                                                    , -     ,
                                                    - ,     1
                                                    , 0     :
                                                    0 ;  00H-
7FH,                                                  RD/WR
                                                    0 ,
0H..7H                                              ,   -   ,
-                                                   , 0     ,
```

```
                                                                0 ,  -
                                                                , -     ,
                                                                - ,     1
                                                                , 1     :
                                                                0 ;  00H-
7FH,                                                                 PSEN
                                                                0 ,
0H..7H                                                          ,   -   ,
-                                                               , -     ,
                                                                1 ,  -
                                                                , -     ,
                                                                - ,     1
                                                                , 1     :
                                                                0 ;  00H-
7FH                                 ,                                VN
REST


                                                                  :     1
                                                                ;

$ A15                                                           ,
(A[11..9])                                                      , IO    ,
RD                                                              , PSEN
                                                                ,MODE   ,
BNK                                                             ,CSBANK
                                                                ,EW     ,
RES                                                             ,FLPRG  :
CSEE                                                            ;     U11
EEPROM/RAM
                                                                1 ,
0H..7H                                                          ,   -   ,
-                                                               , 1     ,
                                                                - ,  0
                                                                , 0     ,
                                                                1 ,     1
                                                                , 0     :
                                                                0 ;  80H-
F9H,                                                                 RD/WR
                                                                1 ,
0H..7H                                                          ,   -   ,
-                                                               , -     ,
                                                                1 ,  0
                                                                , 0     ,
                                                                1 ,     1
                                                                , 1     :
                                                                0 ;  80H-
F9H                                 ,                                VN
REST


                                                                  :     1
                                                                ;

 $ A15      , (A[11..9]), IO , RD, PSEN ,MODE, BNK,CSBANK ,EW     ,
 RES ,FLPRG :  RRD  ;
   - ,  0H..7H   ,  -  ,  0   ,  -   ,- ,  -  ,  0  ,  1 , 1     ,
```

```
   0 :      0 ;  RAM 00H-F9H ,RD
   - ,  0H..7H   ,  -  ,  -   ,  0  ,0 ,  -  ,  -  ,  1 , 1    ,
   1 :      0 ;RAM 00H-F7 ,PSEN
   - ,  0H..7H   ,  -  ,  -   ,  0  ,1 ,  -  ,  0  ,  1 , 1    ,
   1 :      0 ;RAM 00H-F9H ,PSEN
   - ,  0H..7H   ,  -  ,  0   ,  -  ,1 ,  -  ,  0  ,  1 , 1    ,
   1 :      0 ;RAM 00H-F9H ,RD
 REST                                          :  1 ;

 $ A15   ,(A[11..9]), IO, RD   ,PSEN  ,MODE,BNK ,RES   ,    FLPRG
     :   EW ;
     1   ,      5H  ,  1    ,  -   ,   1   , -   ,  -   ,  1   , 0
      :   0  ; FA00H-FBFFH
     1   ,      5H  ,  1    ,  -   ,   1   , 1   ,  -   ,  1   , 1
      :   0  ; FA00H-FBFFH
 REST                                      : 1   ;

 $ A15, (A[11..9]), IO, RD, PSEN,MODE  , BNK , RES ,FLPRG     :
 CSBANK;
   1 , 6H   ,  1 ,  -   , 1   , - ,  -    ,  1 ,   0          : 1
 ;FC00H-FDFFH, RD/WR
   0 , 6H   ,  1 ,  -   , 1   , 0 ,  1    ,  1 ,   1          : 1
 ;7C00H-7DFFH, RD/WR
   1 , 6H   ,  1 ,  -   , 1   , 0 ,  0    ,  1 ,   1          : 1
 ;FC00H-FDFFH, RD/WR
   1 , 6H   ,  1 ,  -   , 1   , 1 ,  -    ,  1 ,   1          : 1
 ;FC00H-FDFFH, RD/WR
 REST                                      :  0 ;

*PINS
 A[8]=1,A[9]=8,A[10]=7,A[11]=6,A[15]=2,
 CSROM=15,CSRAM1=16,CSRAM2=17,CSEE=18,OEROM=3,
 IO=4,FLPRG=5,RES=10,GND=12,MODE=14,RD=11,
 BNK=23,PSEN=9,EW=22,CSBANK=20,RRD=19,VCC=24;

*Fuses
 $6406=BLOWN ;  Enable Clock-Option für Pin 21
*END
```

The Memory map for the EP 419



EP419

The I/O-area splits up as follows:

/CSRTC	FA00H..FA3FH (RTC)
/EW2	FA40H..FA7FH (CAN)
/EW3	FA80H..FABFH (LCD)
/EW4	FAC0H..FAFFH
/EW5	FB00H..FB3FH
/EW6	FB40H..FB7FH
/EW7	FB80H..FBBFH
/EW8	FBC0H..FBFFH

5.2 The Power-On-Jump-Option

Some applications start at the address or 8000h determined by their function instead of the address 0. To still have the possibility of starting a program beginning at the address 8000h after a reset has been applied certain steps have to be followed.
The following chapters describe the available options of power-on-jumps.

5.2.1 Function of the decoder during a power-on

A Hardware-Reset sets the decoder into a special state, where the address area from 0000h to 7FFFh is equal to the memory location from 8000h upward (usually the EPROM). All other Memory locations are disabled at this time. This special state requires a special treatment. That is, the EPROM's first code instruction is a jump command to the address 8003h or where ever above 8003h. After „landing" at the jump address, the shadowed EPROM is removed from the lower memory (0000 - 7FFFh) through the decoder. The RAM-area from 0h to 7FFFh can then be selected as Code and Data area as usual.

5.2.2 Creating your Software applications for Power-On-Jump

During testing your program can be placed below 8000h as usual. If you also use the basic interpreter make sure your program does not exceed the address area above 2000h.

If your program is „ready to burn“ the following must be taken care of:

1. All programs must be linked at addresses greater equal 8000h!
2. The first machine instruction must be a 8000h and be LJMP 8xxxh. 8xxxh is the entry point of your application.
3. The INTEL-HEX-File has to be programmed into a 32 kB-EPROM. Make sure the EPROM-Programmer takes care of the offset in your Intel-Hex file. Otherwise the EPROM programmer will display an error or try to program non-existent EPROM memory (*refer to your EPROM programmer manual for details on how to use offsets*)!

Example:

```
    ORG 8000h ; (or absolute in the Linker-
    Batch file)
    LJMP start
     ..
**  vectors, tables, code etc.    **
     ..
    start:  Program start
or
    ORG 8000h ; (or absolute in the Linker-
    Batch file)
    LJMP 8xxxh

    ORG 8xxxh
    .. startcode ..
```

6 The usage of the SAB80C537-Pins

To achieve the full functionality of the TouchPanel-537 many of the portpins are already used. Because of that some of the interrupt- and timer inputs are occupied. But it is still easy to connect additional Hardware to the TouchPanel-537 if requiring more pins than still available. This is done by disabling certain modules with the belonging jumpers. The following list shows the portpins and the belonging Jumper as well as their usage.

In-/Output	**Usage**	**Jumper**
Port 0.0-0.7	D0-D7	no jumper
Port 1.0	TouchPanel-Interrupt	no jumper
Port 1.1	RS-485 DE	JP17
Port 1.2	Controller-controlled contrast	JP15
Port 1.3	Display OFF	no jumper
Port 1.4	external Keyboard-Interrupt	JP37
Port 1.5	TouchPanel-Ctrl.	no jumper
Port 1.6	Software security device	no jumper
Port 1.7	Bootstrap-button	JP14
Port 2.0-2.7	Addressline HIGH	no jumper
Port 3.0	SERIAL0 RxD0	no jumper
Port 3.1	SERIAL0 TxD0	no jumper
Port 3.2	RS-485 R	JP16[1]
Port 3.2-3.5	STD.P of RTC	JP6[1]
Port 3.2-3.3	/INT CAN-Controller	JP6[1)]+JP41[2]
Port 3.6	/WR	no jumper

[1] : **Attention!** Port 3.2 can be used for SERIAL1 to RS-285, for the CAN-Controller and also for the Real-Time Clock. The jumpers JP6 and JP16 must be placed carefully so that no conflicts occur. If p3.2 is used for the CAN-Controller JP 41 must be closed!

[2] : **Attention!** Port 3.3 can be used for /INT of the CAN-Controllers but also for the Real-Time Clock. The Jumper JP6 has to be placed so that no conflicts occur. If Port 3.3 is used for the CAN-Controller, JP41 has to be closed

In-/Output	**Usage**	**Jumper**
Port 3.7	/RD	no jumper
Port 4.0-4.7	TouchPanel-Input	no jumper
Port 5.0-5.7	TouchPanel-Input	no jumper
Port 6.0	Summer	JP40
Port 6.1	SERIAL1 RxD1	JP10
Port 6.2	SERIAL1 TxD1	JP11
Port 6.3	external Keyboard	JP39
	DATA-IN	
Port 6.4	external Keyboard	JP38
	DATA-OUT	
Port 6.5	external Keyboard	JP36
	CLK-OUT	
Port 6.6	available	no jumper
Port 6.7	available	no jumper
Port 7.0-7.7	available	no jumper
Port 8.0-8.3	available	no jumper

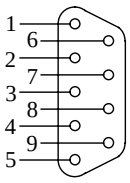
7 The serial ports

The TouchPanel-537 based on the SAB80C537 offers two universal serial Ports: SERIAL0 and SERIAL1.

7.1 SERIAL0

The transmit and receive lines of the first serial ports are connected directly to a transceiver and from there directly to the SUB-D-Connector (X4).

For setting up SERIAL0 no jumpers are required. The serial signals are connected to the SUB-D Connector X4 as follows:



Pin 2: TXD0 (RS-232)
Pin 3: RXD0 (RS-232)
Pin 5: GND

Figure 9: Pin assignment of the SUB-DB9-Connector X4, Front view

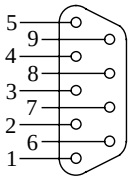
7.2 SERIAL1

7.2.1 Transmit modes of SERIAL1

The signals of SERIAL1 can either be connected via a RS-232-Transmitter or via a RS-485 Transmitter to the Serial connector X6.

The serial signals are connected to the SUB-D Connector X4 depending on transmitter as follows:

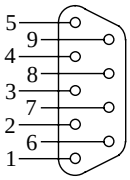
Using a RS-232-Transmitter:



Pin 2: TXD1 (RS-232)
Pin 3: RXD1 (RS-232)
Pin 5: GND

Figure 10: Pin assignment for RS-232, Front view

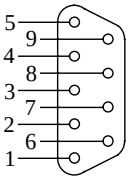
Using a RS-285-Transmitter:



Pin 2: A (RS-285)
Pin 8: B (RS-285)
Pin 5: GND
Pin 6: VCC with the jumper JP22 closed

Figure 11: Pin assignment for a RS-285 Connection, Front view

Transmitting with a CAN-Transmitter:



Pin 2: CAN_Low
Pin 7: CAN_High
Pin 3, 6: CAN_GND
Pin 9: CAN_VCC (nom. 12V)

Figure 12: Pin assignment according to CiA/DS102-1 spec., Front view

7.2.2 Selecting the Transmitting mode for SERIAL1

Transmitting with RS-285 is preferably used over long distances connections and fast transfer rates up to 1Mbps. Also possible with RS-285 it the possibility to connect up to 32 devices at the same time. With RS-232 only 2 Devices can be connected to each other. Also limited is the possible distance and transfer rate. The possible transfer rate decrements very strongly with the distance.
(To give you an Idea: approx. 5 meters distance max. 19600 Baud.) Because of that RS-232 should only be used for a short distance.

To select the desired transfer mode the jumpers 10 - 13 as well as 23 and 24 must be placed accordingly. The position of the jumpers as follows.

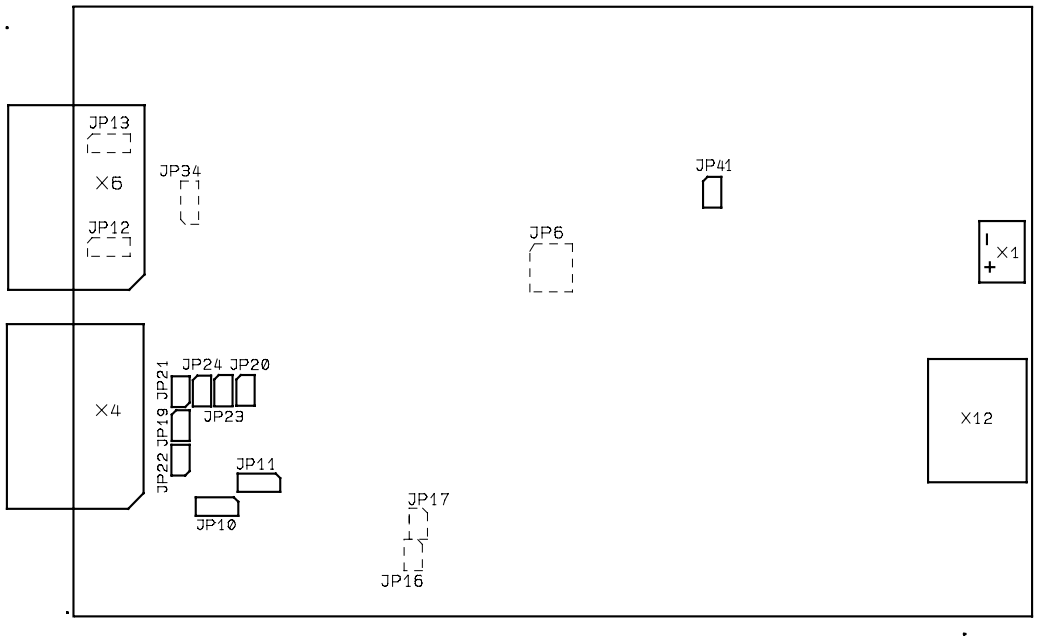


Figure 13: *Position of Jumpers necessary to change the desired transfer mode*

Table for Jumpersetting

SERIAL1 Modesetting (X6)	**RS-232**	**RS-285**	**CAN**
JP6	don't care	don't care	7-8/8-9[1]
JP10, 11	1 - 2	2 - 3	don't care
JP12, 13	1 - 2	open	2 - 3
JP16	open	for µNet[2]	don't care
JP17	open	don't care[3]	don't care
JP19, 20, 21, 22	open	don't care[4]	open
JP23, 24	open	closed	open
JP34	open	1 - 2/open[5]	2 - 3
JP41	don't care	don't care	closed

[1] : **Controlling the CAN-Controller**

The Can-Controller can be controlled through the INT0 or INT1 signals. Because of INT0 also being used for SERIAL1 to RS-285, JP16 must be open while using INT0. Because the RTC is connected to INT0 or INT1 via JP6 you must take care that no conflicts occurs. When using the Can-Controller JP41 must be closed.

[2] : **RS-285 under µNet**

If a RS-285-Network is used under µNet, the RxD-Line must be connected to a bit addressable Port. For that case jumper JP16 must be closed, and data can be read from Portpin 3.2 instead of pin 6.1.
ATTENTION: Portpin 3.2 can also be used for the CAN-Controller and the RTC. If Port 3.2 is used for the serial port jumper JP6 is not allowed on position 5 - 6 or 8 - 9.

[3] : **Controlling the RS-285 transceiver behaviour**

JP17 modifies the „ready to Send" behaviour of the RS-285-transceiver. To avoid disturbances during the power-up of other devices on the Network the transmitter is disabled with the pull-up resistor R9. If desired the transmitter can be enabled by the Controller and Software after power-up. Therefor JP17 must be closed. Now the transmitter can be enabled through Port 1.1.

[4] : **Terminating RS-285-Lines**

If using the Device at the end of the Network, the line has to be terminated. Therefor it is necessary to place a terminating resistor to X6. If the resistors R5,R6,R7 are on-board, they can be used as terminators by setting the Jumpers JP19, JP20, JP21 and JP22.

[5] : **Connecting the powersupply**

If VCC should be available on the X6 connector, Jumper 22 must be closed and Jumper JP34 must be in position 1 - 2. Otherwise jumper JP34 must be open.

7.2.3 SERIAL1 to CAN

Galvanic coupling

If a galvanic coupling is used, the power for the transmitter is supplied by the CAN-bus itself (12 V at Pin 9, GND at Pin 3 and Pin 6 of Connector X6).
The solder-jumpers JR1 and JR3 must be then removed, and the fowling solder bridges JR2 and JR4 must be closed.
If the transmitter is supplied from the systemboard please close JR1, JR3 and JR4 and open JR2.

8 The Chip-Enable-Signals

The TouchPanel-537 supplies 8 freely unable chip enable-signals and are named /EW1 up to /EW8. The CE-signals /EW1 to /EW3 are occupied by the System itself, so that they can not be used for your application anymore.
/EW1 is used for the RTC; /EW2 for the CAN-Controller and /EW3 for the LCD.

The baseaddress of these Controllsignals depend on the used decoder placed in U5.

The /EW signals are only decoded from the addresslines and therefor not free from glitches. This is done to save you some time for necessary following decoding.
If you require a glitchfree decoding, the signals /RD and /WR can be added to the decoding by closing JP26. Default setting is open!

Address range of each /EW signal:

/EW1: Basis + (00H..3FH)	;	Reserved for RTC
/EW2: Basis + (40H..7FH)	;	Reserved for CAN-Controller
/EW3: Basis + (80H..BFH)	;	Reserved for LCD-Controller
/EW4: Basis + (C0H..FFH)		
/EW5: Basis + (100H..13FH)		
/EW6: Basis + (140H..17FH)		
/EW7: Basis + (180H..1BFH)		
/EW8: Basis + (1C0H..1FFH)		

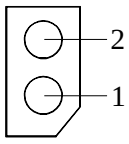
The Basis can be extracted from the description of the logic device and the related /EW-signals.

9 The A/D-converter of the SAB80C537

The integrated A/D-converter(ADC) of the 80C537 used on this board is a real 8-bit converter(80C537A contains a 10 ADC). The controller has 12 analogue inputs which are internally multiplexed 12 to 1. The ADC reference voltage can be programmed internally to different levels, enhancing the sampling resolution. The minimum voltage difference of the programmed internal reference voltage is 1 V. For details refer to the Controller handbook of the 80C537.

The ADC in general can be used for a wide area of applications. Keep in mind that the ADC is no substitute or replacement for a high precision ADC. Check that the converter specification of the controller data sheets meet your requirements.

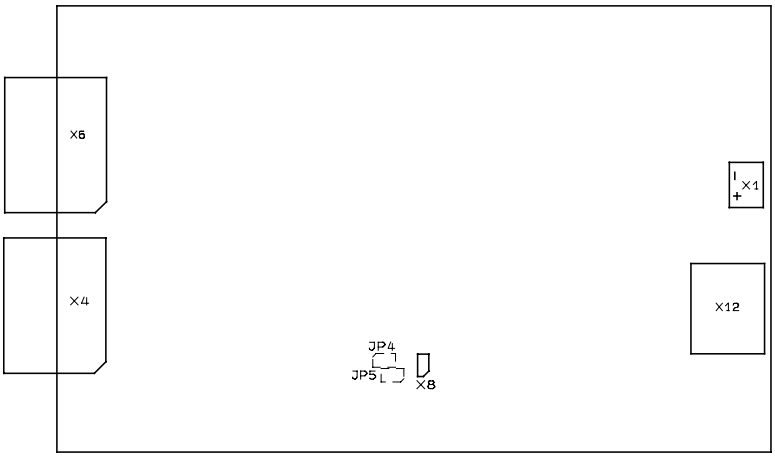
If you are using the ADC it is necessary the controller pins VAREF and VAGND are supplied with a reference voltage of (VAREF)+5 V and (VAGND) 0 V (see data sheet or controller!). The voltage could be VCC and GND or a more precise Voltage source. If using VCC and GND JP4 and JP5 must be closed otherwise they must be open. The external reference voltage may be connected via X8.



Pin 2: VAGND

Pin 1: VAREF

Figure 14: Pin assignment of the external reference voltage input X8



Solderside Componentside

Figure 15: Position of X8 and JP4,JP5

10 The Real-Time Clock (RTC) RTC-72423A

For real-time applications the TouchPanel-537 provides the Real-Time Clock chip RTC-72423 from Seiko/Epson. It supports the following futures:

- internal crystal clock-generation
- direct bus compatible (Access time 120 ns)
- 4-bit wide connection possibility for 8048, 8051 and 8085 Controllers
- adds up a Clock counter(Hour, Minute, Seconds) as well as a Date counter(year, Month, Week and Day)
- optional 12- or 24-hour count
- automatic leap year detection
- maskable interrupts
- Standard pulse-frequency from 1/64 sec., 1 sec., 1 min., 1 h.
- Fault handling mechanism
- low current due to C-MOS

If a Battery is used the Clock runs independent to the TouchPanel-537.

10.1 Accessing the RTC

The RTC is accessed through the I/O-area /EW1 (/EW1: Basis+00h - Basis+3Fh). Access can be achieved by read and write to the xdata-memory (movx @dptr,a; movx a,@dptr) in the address range from Basis+00h.

The base address is depending on the used decoder chip U5.

Addresses of the RTC-72423A Registers:

Time- and Date register:	Basis + 00h up to Basis + 0Ch
Control-register D:	Basis + 0Dh
Control-register E:	Basis + 0Eh
Control-register F:	Basis + 0Fh

(More detail can be found in the included Controller-Handbook from Seiko-Epson.)

10.2 Connecting the RTC to the Controller

The RTC can either be connected to the /INT0 or /INT1 as well as to the Timer inputs T0 and T1.

With the help of jumper JP6 the depending pin of the RTC is connected to the Controller.

STD to:

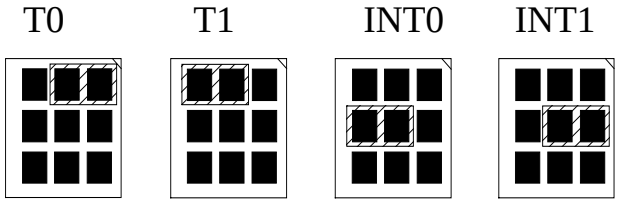


Figure 16: Positions of the Jumpers JP6

2 - 1	Countclock for Timer 0 from RTC
2 - 3	Countclock for Timer 0 from RTC
2 - 4	Interrupt /INT0 from RTC-clocksignal
2 - 6	Interrupt /INT1 from RTC-clocksignal

[1] : **Attention:** INT0 can also be used for SERIAL1 (RS-285) or the CAN-Controller. Therefor JP16 must be open if INT0 is used for the RTC. Additionally JP6 is only allowed on position 7 - 8 to connect the CAN-controller as INT1.

[1] : **Attention:** INT1 can also be used for the CAN-controller. If used for the RTC the jumper JP6 may only used in position 8 - 9 to connect the CAN-Controllers

11 The CAN-Controller

Addressing the CAN-Controller

The CAN-Controller is accessed via the I/O-Area of the module (/EW2: Basis+40h - Basis+7Fh). Direct access can be done by normal read /write commands to xdata-memory (movx @dptr,a; movx a,@dptr) from address Basis+40h and upwards.

The baseaddress of the control signal depends on the used decoder U5. Please refer to the available descriptions of the used decoder.

Addresses of the CAN-Register:

Control Register:	Basis + 40h
Transmit Buffer:	Basis + 4Ah - Basis + 53h
Receive Buffer:	Basis + 54h - Basis + 5Eh

12 The LC-Display

The LCD is a monochrome display of the make LSWWAG8238A from ALPS ELCTRIC. It futures a display area of 96 x 72 mm and a resolution of 320 x 240 pixels. The LCD is backlite which increases the brightness and providing a viewing angle of up to 30° with a high contrast.

12.1 Changing the Contrast

To adjust the Contrast a negative voltage of -8 to -22 V is required. This is supplied by the MAX 749 on-board.

To adjust the contrast there are tree possibilities. First is the software controlled contrast. To enable this, JP 15 must be closed. Closing the jumper connects the Port 1.5 pin to the MAX749. Each positive slope increments a 6-bit counter of the MAX749 which represents a certain contrast providing 64 contrast levels.

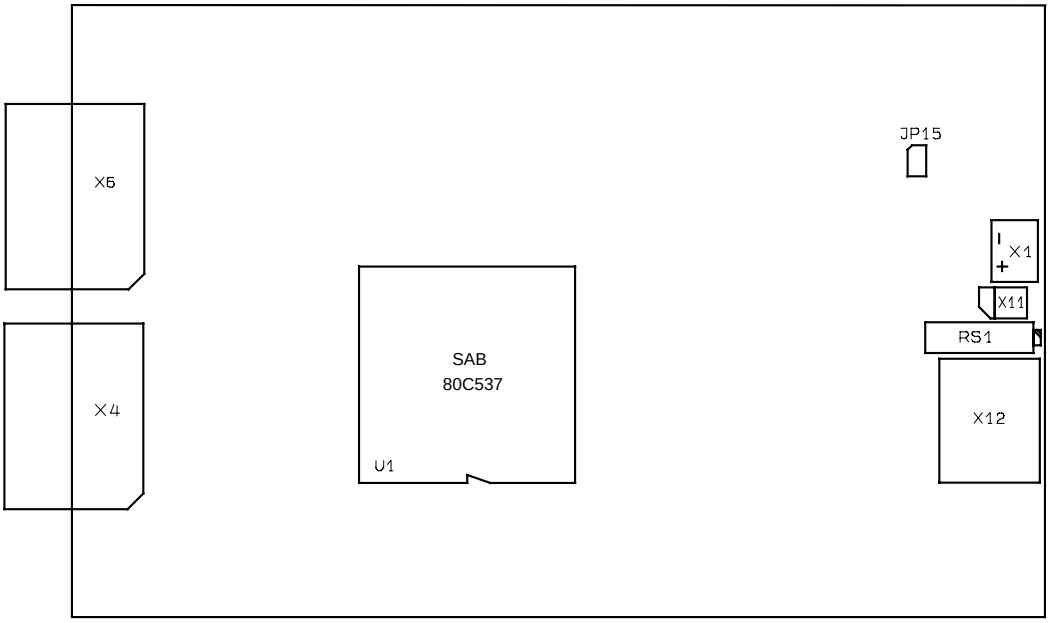


Figure 17: Position of adj. resistor RS1, adj. connector X11 and the Jumper JP15

13 The LCD-Controller

The LCD-controller is based on the SED1330F from Seiko-Epson. It provides a easy to use memory management to handle more than one display layers in the available LCD-memory used for displaying graphics and text. Additionally it has a built-in characterset, which can be expanded to your need by including the graphic capability's

13.1 Memory of the SED1330F

The SED1330F can handle up to 64 kB of memory. The memory can be used as graphic memory as well as charactersets. It supports up to 64 characters with 6 x 16 Pixel on a external RAM as well as a additional 256 characters of the same size in another ROM/RAM. The TouchPanel-537 is equipped with two 32 K RAM's the den LCD-Controller. This means that the alternate characterset have to be initialized after a new program start. The memory is split up as follows:

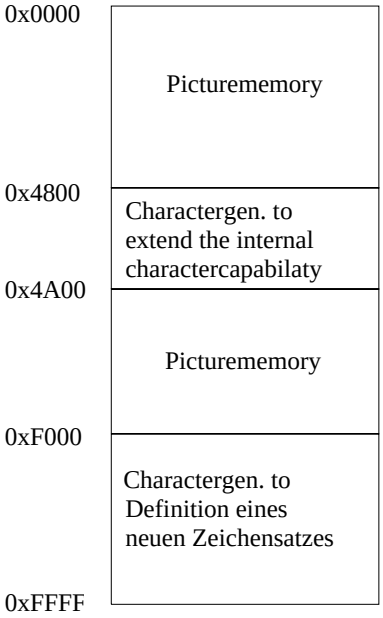


Figure 18: The memory map of the LCD-Controller

13.2 Addressing of LCD-Controller

The Addressing of the LCD-Controller is managed via the I/O-area of the module (/EW3: Basis+80h - Basis+BFh). Direct access to the LCD-Controller can be done by normal read /write commands to xdata-memory (movx @dptr,a; movx a,@dptr) from address base+80h and upwards.

The base address depends on the used decoder! The base address of the control signal depends on the used decoder U5. Please reefer to the available descriptions of the used decoder.

Addresses of the LCD-Registers:

Command Register:	Basis + 80h
Parameter-OUT:	Basis + 81h
Parameter-IN:	Basis + 80h

Due to that a LCD command looks like the following:

1. Command with input parameters:

```
mov DPTR, #(Basis+81H)   ;write the
mov A, comm;             ;command comm
movx                     @DPTR, A
mov DPTR, #(Basis+80H)   ;write the
mov A, parm              ;Parameter parm
movx                     @DPTR, A
```

2. Command with output parameters:

```
mov DPTR, #(Basis+81H)   ;write the
mov A, comm              ;command comm
movx                     @DPTR, A
mov DPTR, #(Basis+81H)   ;read the
movx                     A,@DPTR    ;return value into A
```

For the LCD-commands refer to the SED1330F controller reference manual

14 The TouchPanel

A digital resistive TouchPanel with 10 x 6 keypads constructs the TouchPanel. The size of each key is 11.6 x 9.2 mm. The keypad is readout via Port 4 and 5 as well as INT3 on Port 1.0. The TouchPanel-537-Systemsoftware supplies functions for C and Assembler to make it easy to handle the keypad.

15 External Keyboard

15.1 Supported keyboards

As external Keyboard a IBM-compatible PC-/AT-/ or MF2- Keyboard with German characterset must be used.

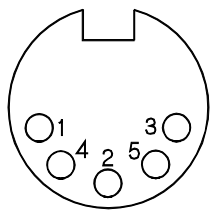
15.2 The characterset

The Keyboard routine supports the entry of ASCII- and Control-characters as well as Keys reached through the Alt-Key and the numberpad.

The Keyboardroutine supports the Caps-Lock, Shift, Ctrl, Alt and Num-Lock keys. The Alt-Gr has no influence on the decoded key. The @ key has therefor been moved to the <F9> Function key. The Functions keys <F7>, <F8> and <F10> are used for ',', '.' and '#', due to differences of some Keyboard manufactures to the original IBM MF2-Keyboards.

15.3 The keyboardinterface

The Keyboard is connected to the TouchPanel-537 with a standard 5-Pin keyboard connector as shown below. The power required by the Keyboard is supplied by the TouchPanel-537 (approx. 100 mA). The communication is done by a synchronous serial interface based on a the Clock- and datalines of the Keyboard. The pinout can be see below.



1 Clock
2 Data
3 NC
4 GND
5 VCC (+5V)

Figure 19: Keyboard interface X12, viewed from the connectorside

To enable the keyboard to generate a interrupt on the TouchPanel-537 the clock signal of the keyboard is connected via a driver to Portpin P1.4. The following data can be read in after that. Because of the bi-directional capabilities two Portpins are required. Therefor Portpin P6.5 is connected to Clock- and Portpin P6.4 is connected with Data. The used driver functions as a safety for the Portpins.

15.4 The Jumpers for the Keyboard-Interface

To use the external keyboard certain Portpin must be connected to the Keyboard interface. This is achieved by closing the jumpers JP36 - JP39.

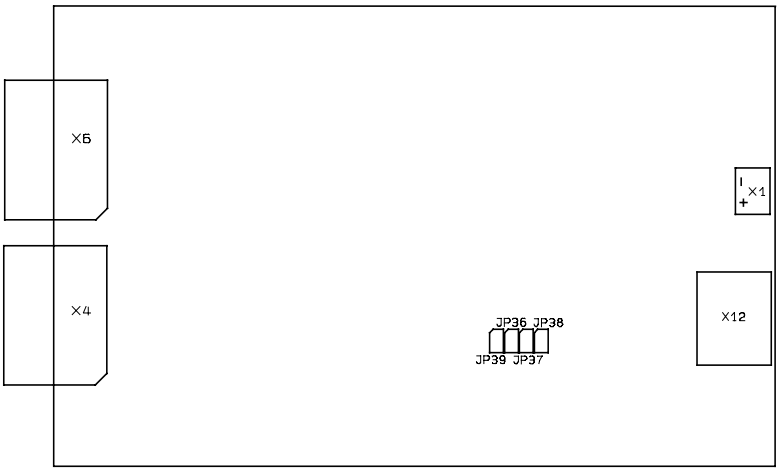


Figure 20: Position of Jumpers for keyboard and connector X12

15.5 The Keyboard driver

With the supplied software for the TouchPanel-537 comes some functions for simple readout of the keyboard. Additional information can be found in the TouchPanel-537 System software manual (*Order. Nr.: L-145*).

16 The Buzzer

To enable Keyboard clicks and other Sound effects the TouchPanel-537 has a buzzer. To use it first of all JP 40 must be closed, connecting the buzzer to Portpin 6.0. A LOW-Level on this Pin switches the buzzer on while a HIGH-level turns the buzzer of.

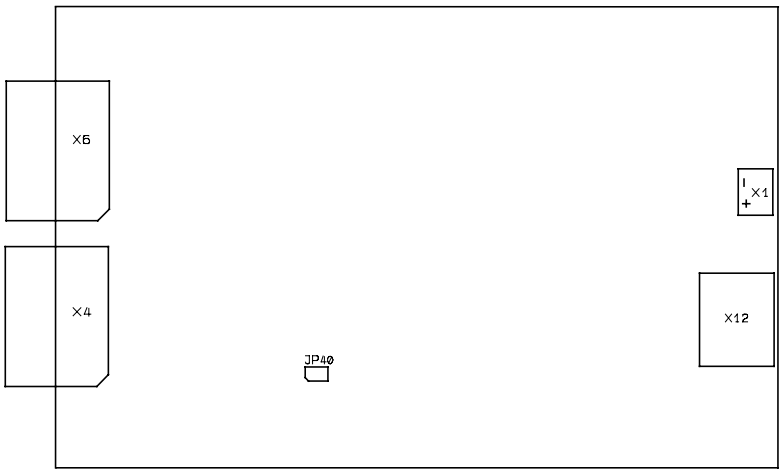


Figure 21: Position of the Jumper JP40

17 Memory configuration

The memory configuration is maintained through the decoder U5. It provides a MODE input allowing to select one of the two desired memory configurations. These modes are named MODE0 and MODE1 via jumper 25 placed on the component side. MODE0 equals a connection to GND (Jumper JP25 pos. 1 - 2), Mode 1 equals a connection to VCC (Jumper JP25 pos. 2 - 3).

The decoder supplies the Enable-Signal for all memory devices of the address range of the SAB80C537. Please check changes of the decoder due to development changes.

A custom made decoder can also be obtain for low cost.

17.1 Memory expansion

Expanding the memory is possible in many different varieties.

17.1.1 Default memory size

The default is a 32 kB Ram placed in U10.
32 kB EPROM on U8 is only supplied together with our Controller software. You can of course also use a 64 kB EPROM in U8. A Flash-version with 128 kB Flash is also available.

Take special care about the jumpers JP27 and JP28!

If delivered with a EPROM in U8 the jumpers are closed according to the EPROM size.
The RAM-Position U9 (SMD) is not used by default.

17.1.2RAM-expansion with U9

U9 can be used for a additional 32 kRam or a 128 kB RAM. U9 shares the address space with U11. The banklatch decides with the help of the signal BNK which memory device is selected. A RAM on U9 with more than 32 kB receives his upper addresslines from the banklatch U15 (B0, B1).
If a 128 kB Flash on U8 is used it also receives its higher Addresslines from the Banklatch (B2).The usage of the Banklatch is described in chapter 20.

17.1.3Expansion on U11

U11 can be used to expand the memory with 8..32 kB DIL-EEPROM. You can also use 32 kB RAM or EPROM as well.
If this is the case, jumpers JP29..JP32 have to be placed accordingly.

U11 can be used as a RAM or a ROM with EPROM or EPROM.

The following table shows how to jumper for the used memory type:

Jumper position for memory usage

EPROM in U8:	**JP27**	**JP28**
8 kB EPROM	1 - 2	1 - 2
32 kB EPROM	1 - 2	2 - 3
64 kByte EPROM	2 - 3	2 - 3
128 kByte Flash	2 - 3	2 - 3

EEPROM/EPROM/ RAM U11	**JP29**	**JP30**	**JP31**	**JP32**
8 kB EEPROM	2 - 3	2 - 3	open	1 - 2
32 kB EEPROM	2 - 3	1 - 2	open	1 - 2
32 kB RAM	2 - 3	1 – 2	open	2 - 3
8 kB EPROM	1 - 2	2 - 3	1 – 2	1 - 2
32 kB EPROM	2 - 5	2 - 3	1 – 2	1 - 2

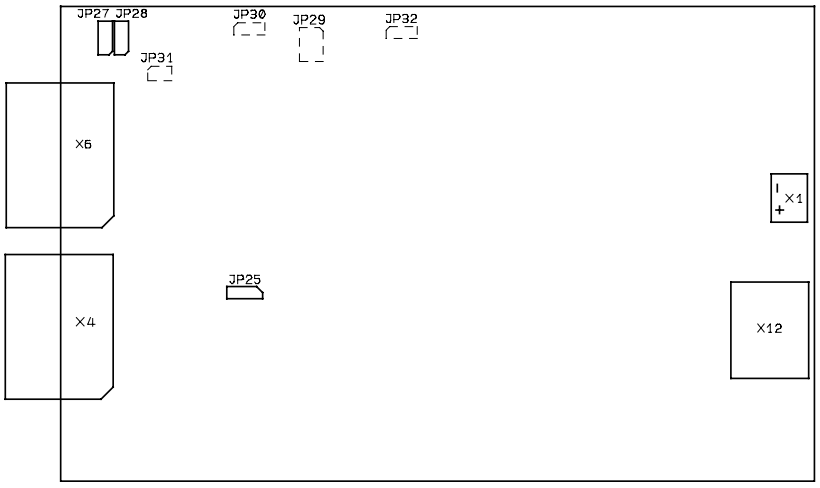


Figure 22: Position of the Jumper to configure the memory used

Hints about memory usage

The SAB80C537 separates data and code memory. Because of that the memory is limited to 128 kB if no bank switching is used. If the specific address decoder is used, code and data can be placed on the same physical address space. The TouchPanel-537 is very flexible in handling this.

Due to safe operation the following points should be pointed out:

- The supported Flash-version of the TouchPanel-537 is upgradable with 128 kB Flash-Memory. We recommend the usage of the AMD 29F010 or similar which are programmable with 5 V.

- Executable code should be stored in EPROM's. Nevertheless a battery backed RAM is used there is still the possibility of a bit toggling making your program and even your watchdog useless. Because of that we strongly recommend EPROM for the „Final CODE".

- If having the Idea of a remote RAM/EEPROM programmable system we recommend the kernel to be EPROM based that supports error detection during transfers and if need be corrected.

- As long as the access time of the EEPROM in not below 200 ns, the code should not be executed from EEPROM because it is to slow.

18 The RAM-write protection and the battery backup

Write protection and battery backup are supplied by U12 and Q2..Q4. This requires a Battery, connected to X2. The current from the battery depends on the quality of the RAM being used and your used Extensions depending on a Battery. Usually a 32 kB RAM requires approx. 1 uA letting a battery last of a few years.

The RAM in U9 and U10 as well as the RTC U7 are supplied by Battery during power-down or VCC going below 4.6 to 4.8 V. U11 may be supplied by VCC or VPD depending on the jumper setting of JP32.

Supply of U11	**JP32**
VPD	2 - 3 ; only RAM
VCC	1 - 2; EPROM or EEPROM

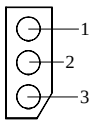
If you forget to place JP 32 correct, a fast discharged battery will be the consequence if a EPROM or EEPROM in U11 is used instead of a RAM.

Function of the battery backup and the write protection

The RAM as well as the RTC are deselected with the /RES-signal. U3 is a uP-Watchchip that is controlled by the supply voltage. If VCC goes below a certain level the Signal /RES is set to Low immediate. U12 passes this Signal on to Q2..Q4, deselecting the RAM disabling the currentflow into the decoder. In Battery-Backup-mode the battery is supplying the RAM and the RTC with available battery voltage VPD.

U12 is used to improve the clearance and level of the /RES-Signal. To ensure the write protection of the RAM the /RESload is limited! After powerup the /RES signal remains low for a short time, to prevent disturbances on the Write lines during powerup.

It should be self-explaining that the write protection is only achieved if the power is supplied or disconnected bouncefree.



1: GND
2: VCC
3: GND

Figure 23: Battery connector X2

19 The RAM-Deselecting for the Power Down/Idle-Mode

Before activating the Power-down or Idle mode the RAM should be deselected. This is achieved with the banklatch U15, bit 1 Signal M-DIS). After Reset the RAM is always selected (M-DIS=LOW). Setting bit 1 (Signal M-DIS) disables the RAM.
Because the banklatch can only be written, a copy of the banklatch should be kept, to know the state of it.

Deselecting the RAM is only useful if running from EPROM.

Example for deselecting the RAM:

```
mov dptr,#banklatch     ; Address of banklatch
mov a,bl_s              ; Backup of Banklatch
orl a,#02H              ; (anl a,#FDH) set bit 1 disable RAM
mov bl_s,a              ; update Backup.
movx @dptr,a            ; Write to latch
```

20 The input ports of the Controller

As can be seen in the controller handbook of the SAB80C537 many functions can be accessed through external circuits:

20.1 Program execution from external/internal ROM

Jumper JP1 has to be Closed if a ROMles version of the 80C5x5 is used. Using the mask-programmable version JP1 selects the source of the code:

Function (CODE memory-Access)				**JP1**
under 2000h internal memory, above 2000h extern	open			
from 0000h to FFFFh only extern			closed	

20.2 Power-Saving-Mode/Watchdog-Enable

Function	**JP2**
PD, IDLE and SLOW-Mode Enable/	2 - 4
Watchdog off	
PD, IDLE and SLOW-Mode Enable	2 - 1
PD, IDLE and SLOW-Mode Disable/	2 - 5
Watchdog start	
PD, IDLE and SLOW-Mode Disable	2 - 6

20.3 Oscillator-Watchdog-Enable

Function of the WD-Oscillator	**JP3**
Watchdog Enabled	open
Watchdog Disabled	closed

21 The Banklatch U15

The Banklatch U15 has the following tasks:

- Deselektion of RAM and EEPROM in the Powerdown mode
- Supply of the Addresssignals A16 for U8
- Supply of the Addresssignals A15 and A16 for U9
- Bankselection between U9 and U11 (decoder depending)

The Latch is coupled with the RESET, so that the outputs are always LOW after a reset.

Access to the latch is achieved through a normal DATA-memory access. Ahead of that the DPTR has to be set to the valid address of the banklatch. Because the Banklatch can only be written, a copy of the banklatch should be kept, to know the state of it.

The address of the banklatch depends on the used address decoder. Please refer to the valid description of the address decoder being used. The referred signal is named CS_BANK.

The following describes the function of the single BITs.

D0: BNK bankselection U9, U11

This Bit has influence on the address decoder U7. It selects together with the address decoder the access from U9 and U11. In the normal mode with D0=LOW the U11 device is accessed. If using a custom solution of the decoder any other function can be used in connection with Bit D0.

D1: M-DIS Memory-Disable

This Bit disconnects the decoder output from the /CE-inputs of U9,U10 and U11.
It is required if using the power saving mode.

D2: FL-PRG

If the Flash-version of the TouchPanel-537 is used bit D2 is required to swap the CODE and XDATA-memory. Because of that the Flash appears in the XDATA area and can therefor be programmed. This option is only supported in the Flash-version and requires the usage of the depending decoder.

D3,D4: Bank-Address of U9

These Bits supply the upper addresslines for U9 as far as the required RAM size is being used otherwise don't care.

D5: Bank-Address of U8

This bit provides the highest addressline of U8 as far as a 128 kByte Flash is being used otherwise don't care.

22 The RESET-Signal

The reset is generated by a watchchip-signal. Possible events to cause a RESET are of course pressing the RESET button but also a Powerfailure (drops).

For your own hardware expansion the available RESET-Signal should not be neglected:

/RES The /RES-Output from U3 is active low and must not be excessively loaded, otherwise the risetime suffers and the Power-On-Jump as well as the RAM-write protection does not work properly. /RES is a Open-Drain-output and may be connected to GND externally.

RES The RES-output of U3 is active high and as mentioned under /RES should not be overloaded to ensure U3 to work properly. If VCC is not available RES shows the battery voltage VPD. RES does not change to High if /RES is manually pulled LOW.

RES2 This Output is active high and may have a stronger load. Its level due to the applied load has no influence on the watchchip U3. The signal is only valid during VCC is in a defined range.

B-RES This output is active high. It behaves similar to RES but passed the level of /RES on! B-RES shows the battery voltage VPD if VCC is low. This enables B-RES to be used on external hardware without VCC being available.

23 Flash utilities

Due to the use of Flash-technology as non-volatile the futures can be used in the TouchPanel-537. These futures include the option of on-board-programming of the Flash-Memory. To handle this you get the Flash utilities already programmed in the on-board Flash and the also required PC-Software. These tools serve as a download-util of your applications into RAM during development and later on into Flash after development. The Flash utilities take care that the FlashTool in the Flash can‘t be overwritten by mistake. The on-board-FlashTool part requires 64 kB of the Flash-Memory. The rest of the memory can be freely used.

23.1 Starting the Flash utilities

To start the FlashTools make sure JP14 (Bootstrap mode) is closed, set up the TouchPanel-537 to the PC via the Serial cable. Start the monitor program Version 2.56C on your PC with *mon51* and the used serial port number.
Press the reset button and the Bootstrap button on the TouchPanel-537 at the same time. Hold the Bootstrap button during the release of the Reset button closed.
Depending on the mode you have selected, two menus will be available.

23.2 Flash-programming

If Jumper JP25 is on position 1 - 2 you are in Mode 0. In this mode the menu for Flash-programming appears. This allows information about the Flash to be displayed, to erase part or all of the Flash-Memory. All menu items should be self-explaining. For your own applications 64 K of Flash are available (*see chapter 5.1.2, “Address decoder EP 419*”). To program the Flash only Intel-hexfiles should be used.
After downloading the Program it can be started by applying a simple reset.

Attention:
The Flash utilities take care by Software only that the FlashTools themselves can not erased. This enables you to program your Hardware many times.

23.3 RAM-Download

During development we recommend you to use the RAM for your testing and debugging due to the fact that a flash is limited to approx. 100.000 erase-cycles. To enable this set Jumper JP25 on pos. 2 - 3. This set up the TouchPanel-537 into Mode 1. In this memory model the Menu for RAM-Download appears. This allows you load a program into ram and to set-up the start address of your program. Because of that future you can keep more than one program in RAM and execute one by setting up the proper entry address. The software may be debugged using the monitor program from Keil Elektronik GmbH.
To use this future the monitor program (mon51.hex) has to be loaded at address E900H. Make sure that your Program only used memory locations below E900h and that the memory is defined as von-Neumann (*see chapter 5.1.2, "Address decoder EP 419*"). Using the Keil-monitor 58K for your Software is available. If not using the monitor you may use up to 62K due to the IO mapped area.
After you have loaded your program in to ram and have set the start address you may start the program by a normal reset.

24 Appendix

24.1 Troubleshooting

a Do *LC-Display* appears
Check contrast-setting of the jumper, the adj. resistor next to the power supply inputs(RS1)

b The *Buzzer* is not working:
Make sure solderjumper JP40 next to the Buzzer is closed.

c Your *Program* in a *64K EPROM* does not work:
The Address decoder P386 only supports EPROMS up to 32K. In this case you will need a custom solution of the decoder. For advice call our Hot-line.

d The *CAN Interface* does not work:
Check JP41 is closed. If INT1 (JP6 on 7 - 8) is used. JP6 is not allowed in pos. 4 - 5 additionally. If INT0 is used (JP6 on 8 - 9) JP16 must be open and JP6 may not be jumpered on position 5 - 6 at the same time.

e The *RTC* does not work:
Make sure that if INT1 (JP6 on 4 - 5) is used JP6 is not allowed on pos. 7 - 8 at the same time. If using INT0 (JP6 on 5 - 6) JP16 must be open and JP6 may not be in pos. 8 - 9 at the same time.

f *µ-Net* not working:
Make sure JP16 is closed. Also make sure that INT0 is not being used by any other device such as the RTC or the CAN-controller(JP6 not on pos. 5 - 6 or 8 - 9)

g The *Flash utilities* can not be started:
Make sure solderjumper JP14 is closed

h The *external keyboard* does not work:
Make sure solderjumper JP36 - JP39 are closed

Index

A

A/D-Converter.....43
Accessing the RTC.....45
Address decoder.....20
Addressing of LCD-Controller .50
Appendix.....71

B

Banklatch.....66
battery backup.....62
Buzzer.....56

C

CAN.....37, 41
  Addressing the
    CAN-Controller.....47
Galvanic coupling.....41
Changing the Contrast.....48
Chip-Enable.....42
Connecting the power supply....40
Connecting the RTC to the
  Controller.....46
Controlling the
  CAN-Controller.....40
Controlling the RS-285
  transceiver behaviour.....40

D

Dimensions.....6

E

External Keyboard.....54

F

Features.....3
Flash utilities.....69

G

Getting started.....7

I

Input.....34
Input ports of the Controller.....65
Introduction.....1

J

Jumper.....14
Jumper groups.....14
Jumper position for
  memory usage.....60
Jumper setting
  address decoder.....18
  buzzer.....19
  Controller settings.....19
  memory equipment.....18
Jumper setting
  External Keyboard.....55
  RTC.....46
Jumper setting for contrast.....17
Jumper setting for external
  Keyboard.....17
Jumper setting
  battery backup.....18

K

Keyboard driver.....55

L

LCD-Controller 49
LC-Display 48
  Changing the Contrast 48

M

Memory configuration 58
Memory expansion 58
Memory organisation 20

O

Output 34

P

Placement of jumper 15
Port connectors 11
Portpins 34
Possibilities for connecting
  external Peripheries 10
Power supply 6
Power-On-Jump 31

R

RAM-Deselecting 64
RAM-write protection 62
Real-Time Clock 45
Reset-Signal 68
RS-232 37
RS-285
  under µNet 40
RS-485 37

S

Schematics 4
Serial Port
SERIAL0 36
SERIAL1 37
  Selecting the Transmitting
    mode 39
  to CAN 37, 41
  Transmit modes 37
Setting of the jumper
  A/D-Converter 17
Setting of the jumper 16
Signal connectors 11
strip connectors 10

T

Terminating RS-285-Lines 40
TouchPanel 52

Document: **TouchPanel-537**
Document number: **L-146e_1, January 1997**

How would you improve this manual?

Did you find any mistakes in this manual? page

Submitted by:
Customer number: _____

Name: _____

Company: _____

Address: _____

_____

Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

Published by

PHYTEC

Ordering No. L-146e_1
Printed in Germany