phyCORE-AT91M55800A

Hardware Manual

Edition February 2003

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Preface

This phyCORE-AT91M55800A Hardware Manual describes the board's design and functions. Precise specifications for the Atmel AT91M55800A microcontroller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-AT91M55800A

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-AT91M55800A is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit as well as selected 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-AT91M55800A belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-AT91M55800A is a subminiature (60 x 53 mm) insert-ready Single Board Computer populated with the ATMEL AT91M55800A microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the ATMEL AT91M55800A. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-AT91M55800A.

The phyCORE-AT91M55800A offers the following features:

- subminiature Single Board Computer (60 x 53 mm) achieved through modern SMD technology
- populated with the ATMEL AT91M55800A microcontroller (BGA-176 packaging)
- improved interference safety achieved through multi-layer PCB technology and dedicated Ground pins
- controller signals and ports extend to two 100-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- 16-bit, demultiplexed bus mode
- 32 MHz clock frequency (31.25 ns instruction cycle)
- 128 MByte address space
- 1 MByte (up to 16 MByte) on-board Flash[1]
- on-board Flash programming, no dedicated Flash programming voltage required through use of 3.3 V Flash devices
- 512 kByte (up to 8 MByte) RAM on-board, max. 2 MByte at 0 wait states[1]
- optional Infineon 82C900 TwinCAN controller
- up to two Philips 82C251 CAN transceiver, or Infineon TLE6250
- RS-232 transceiver for three serial interfaces
- optional CS8900A Ethernet controller with EEPROM
- 2 kByte (up to 8 kByte) SPI-EEPROM[1]
- up to 6 free Chip Select signals for easy connection of peripherals
- one operating voltage for core & peripherals, 3.3 V, typ. <150 mA
- additional operating voltage for CAN applications only, 5 V, typ. <100 mA

[1] : Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

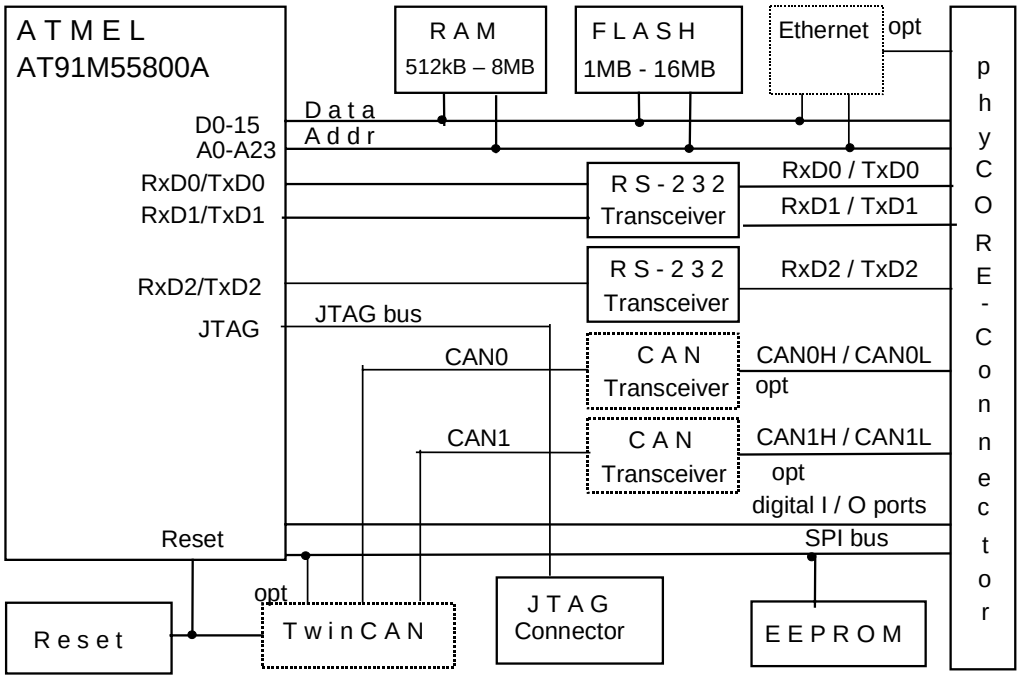


Figure 1: Block Diagram phyCORE-AT91M55800A

1.2 View of the phyCORE-AT91M55800A

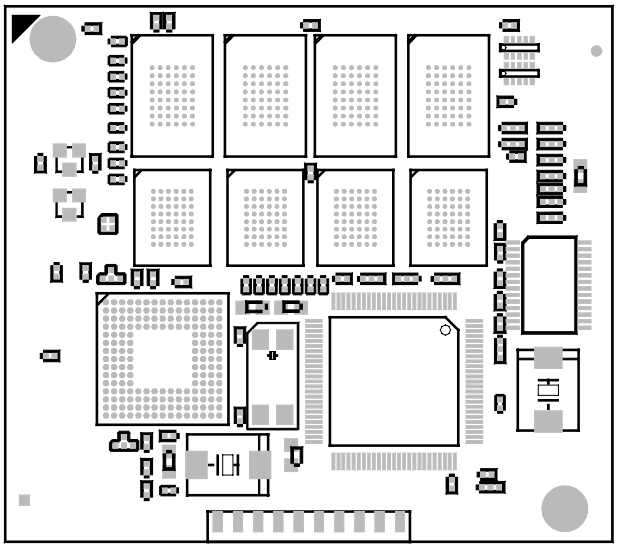


Figure 2: Top View of the phyCORE-AT91M55800A

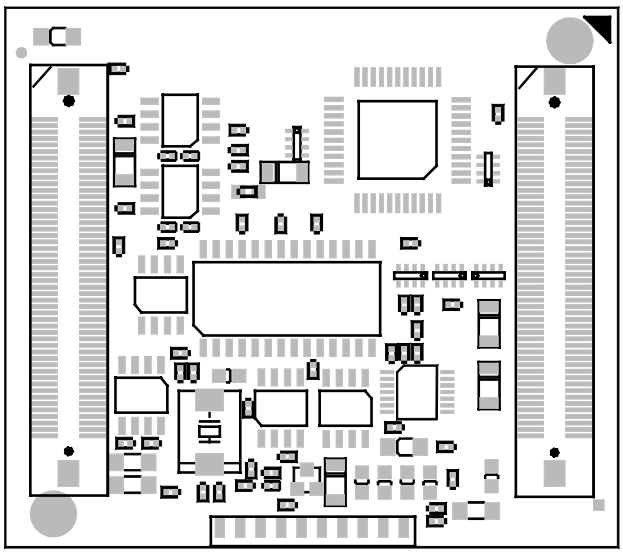


Figure 3: Bottom View of the phyCORE-AT91M55800A

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-AT91M55800A to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-AT91M55800A (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-AT91M55800A marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-AT91M55800A with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a crossview of the phyCORE module showing these phyCORE-connectors mounted on the underside of the module's PCB.

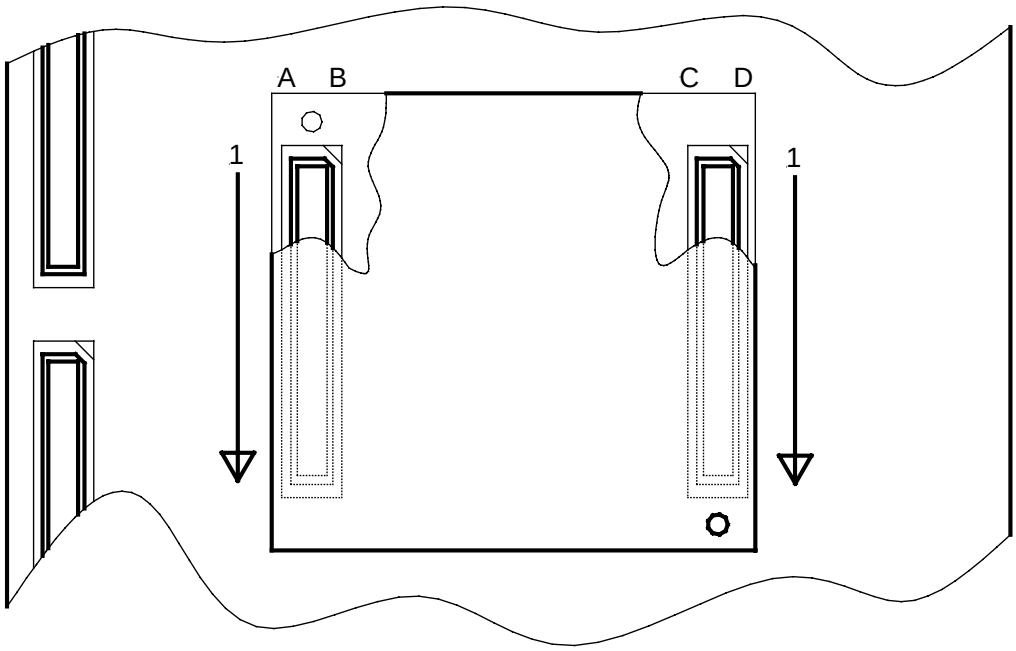


Figure 4: Pinout of the phyCORE-Connector (Top View, with Cross Section Insert)

Many of the controller port pins accessible at the connectors along the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector , as well as descriptions of possible alternative functions. *Please refer to the Atmel phyCORE-AT91M55800A User's Manual/Data Sheet for details on the functions and features of controller signals and port pins.*

Pin Number	Signal	I/O	Description
Pin Row X1A			
1A	CLKIN	I	Optional external clock generator (only in if Jumper J36 is closed)
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A	GND	-	Ground 0 V
3A	PA10	I/O	External Interrupt 1 Input (I)
4A	PA12	I/O	External Interrupt 3 Input (I)
5A	/CS0	O	Chip Select #0
6A	/CS2	O	Chip Select #2
8A	/WR	O	/WR signal of the microcontroller
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A	A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23	O	Address line of the microcontroller
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A	D1, D2, D4, D7, D9, D10, D12, D15	I/O	Data line of the microcontroller
34A	/WAIT	I	Microcontroller WAIT signal input
35A	/CS4	O	Chip Select #4
36A	/CS6	O	Chip Select #6
38A, 39A 40A, 41A 43A	PB9, PB11, PB12, PB14, PB17	I/O	Port B of the microcontroller (*see corresponding Data Sheet*)
44A	PB19	I/O I	Port B19 of the microcontroller TCLK0 Timer0 external clock
45A	PB20	I/O	Port B20 of the microcontroller Timer0 I/O pin A
46A	PB22	I/O I	Port B22 of the microcontroller TCLK1 Timer1 external clock
48A	PB25	I/O I	Port B25 of the microcontroller TCLK2 Timer2 external clock
49A	PB27	I/O	Port B27 of the microcontroller Timer2 I/O Pin B
50A	NC	-	Not connected. These contacts should remain unconnected on the target hardware side.

Pin Number	Signal	I/O	Description
Pin Row X1B			
1B	MCKO	O	CLKOUT system clock output
2B, 3B	PA9, PA11	I/O	Port A9 of the µC, external interrupt 0 input (I) Port A11 of the µC, external interrupt 2 input (I)
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B	GND	-	Ground
5B	/CS1	O	Chip Select #1
6B	/CS3	O	Chip Select #3
7B	/RD	O	/RD signal of the microcontroller
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B	A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22	O	Address line of the microcontroller
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B	D0, D3, D5, D6, D8, D11, D13, D14	I/O	Data line of the microcontroller
33B	/UB	O	/UB Upper Byte Select
35B	/CS5	O	Chip Select #5
36B	/CS7	O	Chip Select #7
37B, 38B, 40B, 41B, 42B	PB8, PB10, PB13, PB15, PB16	I/O	Port B of the microcontroller (*see corresponding Data Sheet*)
43B	PB18	I/O I	Port B18 of the microcontroller Boot mode select input
45B	PB21	I/O	Port B21 of the microcontroller Timer0 I/O pin B
46B	PB23	I/O	Port B23 of the microcontroller Timer1 I/O pin A
47B	PB24	I/O	Port B25 of the microcontroller Timer1 I/O pin B
48B	PB26	I/O	Port B27 of the microcontroller Timer2 I/O pin A
50B	PB5	I/O I	Port B5 of the microcontroller External interrupt 6 input (I)

Pin Number	Signal	I/O	Description
Pin Row X1C			
1C, 2C	VCC	-	Voltage input +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C	GND	-	Ground 0 V
4C, 5C	VCC2	-	Voltage input +5 VDC
6C	VBAT	I	Battery input for back-up of RTC and optional buffering of RAM
8C	/WDOVF	O	Watchdog timer output
9C	PA17	I/O I/O	Port A17 of the microcontroller SCK1 external serial clock 1
10C	/RESET	O	/RESET output of the phyCORE-AT91M55800A
11C	/SHDN	O	Shutdown signal of the microcontroller
13C	PA2	I/O	Port A2 of the microcontroller - Timer3 I/O pin B
14C	PA4	I/O	Port A4 of the microcontroller - Timer4 I/O pin A
15C	PA5	I/O	Port A5 of the microcontroller - Timer4 I/O pin B
16C	PA7	I/O	Port A7 of the microcontroller - Timer5 I/O pin A
18C	CAN-H1	I/O	Differential CANH line of second CAN transceiver
19C	SCK0	I/O	External serial clock 0
20C	WAKEUP	I	Wakeup input
21C	RxD1_RS232	I	Input of the second serial interface of the phyCORE-AT91M55800A, RS-232 level
23C	TxD1_RS232	O	Output of the second serial interface of the phyCORE-AT91M55800A, RS-232 level
24C	RxD2_RS232	I	Input of the third serial interface of the phyCORE-AT91M55800A, RS-232 level
25C	TxD2_RS232	O	Output of the third serial interface of the phyCORE-AT91M55800A, RS-232 level
26C	/PCS0	I/O	SPI Chip Select 0
28C	MOSI	I/O	Master-Our-Slave-In
29C	/PCS2	O	SPI Chip Select 2
30C	/PCS3	O	SPI Chip Select 3
31C	PB1	I/O	Port B1 of the microcontroller
33C	LINK_LED	O	LINK-LED output for Ethernet interface
34C	LAN_LED	O	LAN LED output for Ethernet interface
35C	RxD-	I	Negative Rx input of the Ethernet interface
36C	TxD-	O	Negative Tx output of the Ethernet interface
38C	TDI	I	Data input JTAG interface
39C	/TRST	I	Reset input JTAG interface
40C	TCK	I	Clock input JTAG interface
41C	PA8	I/O	Port A8 of the microcontroller Timer5 I/O pin B
42C, 47C	VAGND	-	Analog Ground of the microcontroller
43C	DA0	O	Analog output 0 of the microcontroller
44C, 45C	AD1TRIG, AD0TRIG	I	Trigger inputs of the A/D converter
46C, 48C, 49C, 50C	AD6, AD3, AD1, AD0	I	Analog inputs of the microcontroller

Pin Number	Signal	I/O	Description
Pin Row X1D			
1D, 2D	VCC	-	Voltage input +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D. 39D	GND	--	Ground 0 V
4D, 5D, 7D, 8D	NC	-	Not connected. These contacts should remain unconnected on the target hardware side.
6D	VPD	O	Output of back-up voltage supply for buffering of external components
10D	/RESIN	I	/RESET input of the phyCORE-AT91M55800A
11D	PA0	I/O I	Port A0 of the microcontroller TCLK3 Timer3 external clock
12D	PA1	I/O	Port A1 of the microcontroller Timer3 I/O pin A
13D	PA3	I/O I	Port A3 of the microcontroller TCLK4 Timer4 external clock
14D	PA6	I/O I	Port A6 of the microcontroller TCLK5 Timer5 external clock
16D	RxD0	I	Input of the first serial interface, TTL level
17D	TxD0	O	Output of the first serial interface, TTL level
18D	CAN-L1	I/O	Differential CANL line of the 2nd CAN transceiver
20D	CAN-L0	I/O	Differential CANL line of the first CAN transceiver
21D	CAN-H0	I/O	Differential CANH line of the first CAN transceiver
22D	RxD0_RS232	I	Input of the first serial interface, RS-232 level
23D	TxD0_RS232	O	Output of the first serial interface, RS-232 level
25D	SCK2	I/O	External serial clock 2
26D	/PCS1	O	SPI Chip Select 1
27D	MISO	I/O	Master-In-Slave-Out
28D	SPCK	I/O	Clock input SPI interface
30D, 31DD	PB0, PB2	I/O	Port B of the microcontroller
32D	PB3	I/O I	Port B3 of the microcontroller Ext. interrupt 4 input
33D	PB4	I/O I	Port B4 of the microcontroller Ext. interrupt 5 input (I)
35D	RxD+	I	Positive Rx input of the Ethernet interface
36D	TxD+	O	Positive Tx output of the Ethernet interface
37D	JTAGSEL	I	JTAG-MODE input (ICE or JTAG-MODE)
38D	TDO	O	Data output JTAG interface
40D	TMS	I	JTAG interface select input
41D	PA13	I/O I	Port A13 of the microcontroller Fast ext interrupt input
42D	DAVREF	I	Reference voltage input for D/A converter
43D	DA1	O	Analog output 1 of the microcontroller
44D, 49D	VAGND	-	Analog Ground
45D, 46D, 47D, 48D	AD7, AD5, AD4, AD2	I	Analog inputs of the microcontroller
50D	VAREF	I	Reference voltage input for A/D converter

Table 1: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-AT91M55800A has 40 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and *Figure 7* indicate the location of the jumpers on the board. All solder jumpers are located at the top side (microcontroller side) of the module.

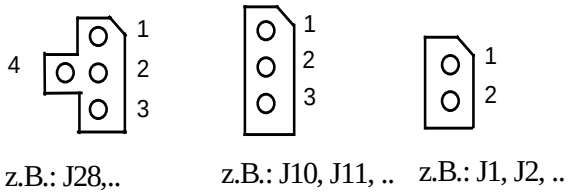


Figure 5: Numbering of the Jumper Pads

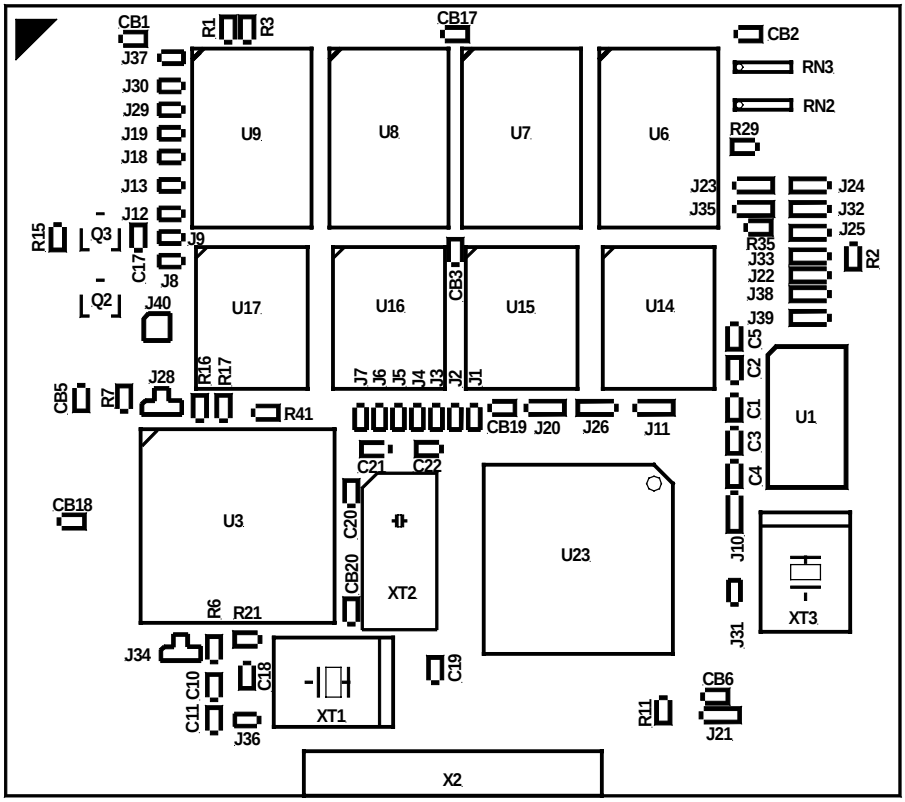


Figure 6: Location of the Jumpers (Top View)

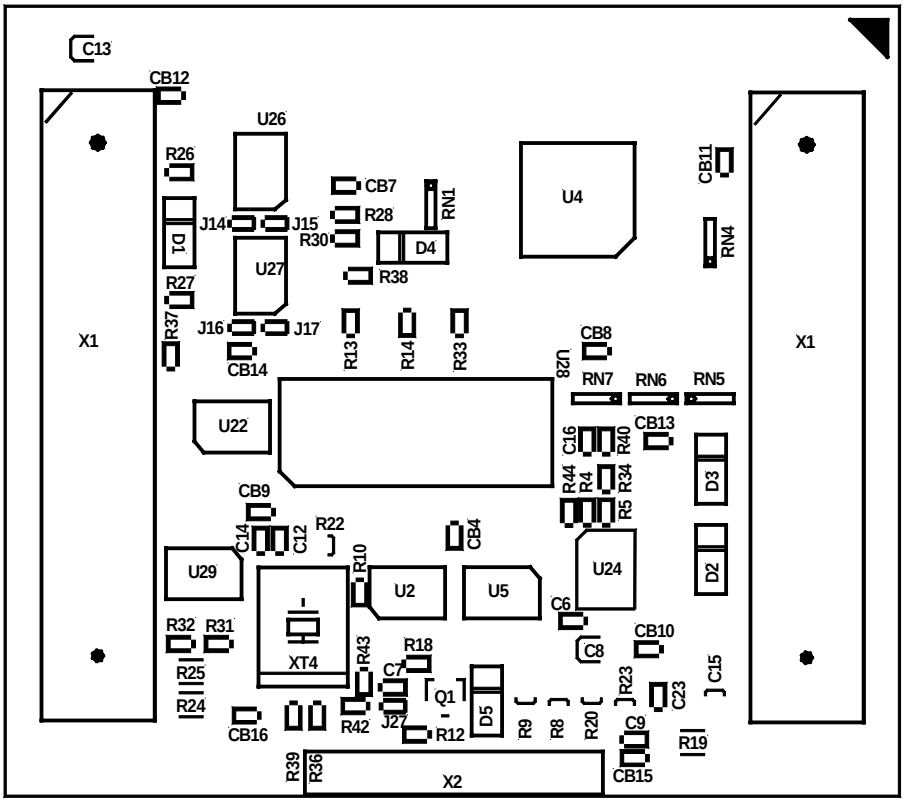


Figure 7: Location of the Jumpers (Bottom View)

The jumpers (J = solder jumper) have the following functions:

	Default Setting[1]		**Alternative Setting**	
J1	(closed)	PA15 as TxD0 connected with RS-232 transceiver	(open)	PA15 of the µC available as standard I/O or TxD0_TTL at pin X1D17
J2	(closed)	PA16 as RxD0 connected with RS-232 transceiver	(open)	PA16 of the µC available as standard I/O or RxD0_TTL at pin X1D16
J3	(closed)	PA23 as SPCK (SCLK) connected with SPI bus	(open)	PA23 of the µC available as standard I/O at pin X1D28
J4	(closed)	PA24 as MISO (MRST) connected with SPI bus	(open)	PA24 of the µC available as standard I/O at pin X1D27
J5	(closed)	PA25 as MOSI (MTSR) connected with SPI bus	(open)	PA25 of the µC available as standard I/O at pin X1C28
J6	(closed)	PA26 as /PCS0 connected with SPI bus	(open)	PA26 of the µC available as standard I/O at pin X1C26
J7	(closed)	PA27 as /PCS1 connected with SPI bus	(open)	PA27 of the µC available as standard I/O at pin X1D26
J8	(closed)	PA9 as IRQ0 (INT_CAN) connected with SPI bus	(open)	PA9 of the µC available as standard I/O at pin X1B2
J9	(closed)	PA10 as IRQ1 (RDY_CAN) connected with SPI bus	(open)	PA10 of the µC available as standard I/O at pin X1A3
J10	(1 + 2)	PA21 as TxD2 with RS-232 level available at pin X1C25	(2 + 3)	PA21 of the µC available as standard I/O or TxD2_TTL at pin X1C25
J11	(1 + 2)	PA22 as RxD2 connected with RS-232 transceiver	(2 + 3)	PA22 of the µC available as standard I/O or RxD2_TTL at pin X1C24
J12	(open)	RAM configuration input 1 of the CPLD U4 connected to VCC via pull-up	(closed)	RAM configuration input 1 of the CPLD U4 connected to GND
J13	(open)	RAM configuration input 2 of the CPLD U4 connected to VCC via pull-up	(closed)	RAM configuration input 2 of the CPLD U4 connected to GND

1: Applies to standard modules without optional features.

	Default Setting		**Alternative Setting**	
J14	(open)	CAN0 transmit line connected with CAN transceiver U26	(closed)[1]	CAN0 transmit line with TTL level available at pin X1D21, for external opto-isolated CAN transceiver connection
J15	(open)	CAN0 receive line connected with CAN transceiver U26	(closed)[1]	CAN0 receive line with TTL level available at pin X1D20, for external opto-isolated CAN transceiver connection
J16	(open)	CAN1 transmit line connected with CAN transceiver U27	(closed)[2]	CAN1 transmit line with TTL level available at pin X1C18, for external opto-isolated CAN transceiver connection
J17	(open)	CAN1 receive line connected with CAN transceiver U27	(closed)[2]	CAN1 receive line with TTL level available at pin X1D18, for external opto-isolated CAN transceiver connection
J18	(open)	Flash configuration input 1 of the CPLD U4 connected to VCC via pull-up	(closed)	Flash configuration input 1 of the CPLD connected to GND
J19	(open)	Flash configuration input 2 of the CPLD U4 connected to VCC via pull-up	(closed)	Flash configuration input 2 of the CPLD connected to GND
J20	(2 + 3)	DAVREF (external) connected with D/A converter reference voltage input	(1 + 2)	VCC connected with D/A converter reference voltage input
J21	(2 + 3)	ADVREF (external) connected with A/D converter reference voltage input	(1 + 2)	VCC connected with A converter reference voltage input
J22	(1 + 2)	Reset for battery back-up via RC circuitry	(2 + 3)	Reset for battery back-up connected to /RESET signal
J23	(open)	82C251 CAN transceiver populates U27 or U27 not populated	(1 + 2) (2 + 3)	TLE6250V33 populates U27 TLE6250V5 populates U27
J24	(1 + 2)	TWIN-CAN controller supplied by VCC2	(2 + 3)	TWIN-CAN controller supplied by VCC

[1] : **Note!** Use only if CAN transceiver is **NOT** populated at U26.
[2] : **Note!** Use only if CAN transceiver is **NOT** populated at U27.

	Default Setting		**Alternative Setting**	
J25	(1 + 2)	VCCRAM connected with VCC	(open) (2 + 3)	No power supply for RAM devices VCCRAM connected with VBAT, for external supply via battery
J26	(2 + 3)	Adresse line A0 connected with /SBHE input of the CS8900A	(1 + 2)	configured /CS signal connected with /SBHE input of the CS8900A, *see J28*
J27	(closed)[1]	/RESIN connected with U5, U2 not populated (CAN circuitry not available)	(open)	/RESIN connected with U2 (CAN circuitry populates the module
J28	(open)[2]	/CS2, /CS3 and /CS4 freely available at pins X1A6, X1B6 and X1A35	(1 + 2)[3] (2 + 4) (2 + 3)	/CS2 selects CS8900A /CS3 selects CS8900A /CS4 selects CS8900A
J29	(closed)[4]	/CS0 connected with /CSF0 (only if CPLD U4 is not populated)	(open)[5]	/CS0 of the controller connected with CPLD U4, CPLD generates /CSF0 - /CSF7 signals
J30	(closed)[3]	/CS1 connected with /CSR0 (only if CPLD U4 is not populated)	(open)[4]	/CS1 of the controller connected with CPLD U4, CPLD generates /CSR0 - /CSR7 signals
J31	(open)	EEPROM Write Protect function disabled	(closed)	EEPROM Write Protect function enabled
J32	(1 + 2)	I/O pins at port A/B operate with VCC (3.3 V)	(2 + 3)	I/O pins at port A/B operate with VCC2 (5 V)
J33	(open)	/RESET_CAN not connected	(1 + 2) (2 + 3)	PB0 of the controller connected with /RESET_CAN for wake-up from power-down mode Module's /RESET signal connected with /RESET_CAN
J34	(open)[1]	PA11 – PA13 freely available at pins X1B3, X1A4 and X1D41	(1 + 2)[2] (2 + 4) (2 + 3)	CS8900A IRQ routed to /IRQ2 CS8900A IRQ routed to /IRQ3 CS8900A IRQ routed to FIQ
J35	(open)	82C251 CAN transceiver populates U26 or U26 not populated	(1 + 2) (2 + 3)	TLE6250V33 populates U26 TLE6250V5 populates U26

1 : Default if minimum configuration of the phyCORE-AT91M55800A is used.

2 : Default if Ethernet controller is not populated.

3 : Default if Ethernet controller is populated.

4 : Default if minimum configuration of the phyCORE-AT91M55800A is used.

5 : Default on all other configuration options of the phyCORE-AT91M55800A.

	Default Setting		**Alternative Setting**	
J36	(open)	CLKIN (pin X1A1) not connected with XIN of the microcontroller	(closed)	CLKIN as external clock input connected with XIN of the µC (use only if on-board quartz crystal is not populated)
J37	(closed)	RY//BY signal from the Flash connected with /WAIT input of the µC	(open)	RY//BY signal from the Flash not connected with micro-controller /WAIT input
J38	(1 + 2)	PA19 as RxD1 connected with RS-232 transceiver and available at pin X1C21	(2 + 3)	PA19 of the µC available as standard I/O or RxD1_TTL at pin X1C21
J39	(1 + 2)	PA18 as TxD1 with RS-232 level available at pin X1C23	(2 + 3)	PA18 of the µC available as standard I/O or TxD1_TTL at pin X1C23
J40	(1 + 2) (3 + 4)	/LB and /UB signals configured for accessing fast SRAM devices	(1 + 3) (2 + 4)	/LB and /UB signals configured for accessing standard SRAM devices

Table 2: Jumper Settings

3.1 J1, J2 First Serial Interface

Jumper J1 and J2 connect the signals of the first synchronous/ asynchronous serial interface to the on-board RS-232 transceiver. The interface signals are then available with RS-232 level at the phyCORE-connector pins X1D22 (RxD0) and X1D23 (TxD0). If the jumpers are opened, the applicable controller pins PA15 and PA16 can be used with their alternative functions or the serial interface signals are available with their TTL level at phyCORE-connector pins X1D17 and X1D16.

If the jumpers are closed we recommend **not** to use the interface signals with their TTL level as this will cause damage to the on-board components.

The following configurations are possible:

Signal Configuration	J1	J2
TxD0 and RxD0 with RS-232 level	closed*	closed*
PA15 and PA16 as I/O pin or TxD0 and RxD0 interface signals with TTL level	open	open

* = Default setting

Table 3: J1, J2 First Serial Interface Configuration

3.2 J3, J4, J5, J6, J7, J8, J9 SPI Interface

Jumpers J3 thru J9 seperate the SPI interface signals of the microcontroller from the on-board SPI bus. The on-board EEPROM (U29) and the Twin-CAN controller (U28) are connected to the SPI bus. If the jumpers remain open, then the applicable controller pins PA9, PA10 and PA23 thru PA27, can be used with their alternative functions or the SPI signals are available at phyCORE-connector pins X1B2, X1A3, X1D28, X1D27, X1C28, X1C26, X1D26.

The following configurations are possible:

Function	J3	J4	J5
on-board SPI bus connected (SCLK, MRST and MTSR)	closed*	closed*	closed*
on-board SPI bus disconnected	open	open	open

* = Default setting

Table 4: J3, J4, J5 SPI Interface Signal Configuration

Function	J6	J7	J8	J9
/PCS_0 connected with Twin-CAN	closed*			
/PCS_0 disconnected from Twin-CAN	open			
/PCS_1 connected with E²PROM		closed*		
/PCS_1 disconnected from E²PROM		open		
PA9 connected with CAN interrupt			closed*	
PA9 disconnected from CAN interrupt			open	
PA10 connected with Ready-CAN				closed*
PA10 disconnected from Ready-CAN				open

* = Default setting

Table 5: J6, J7, J8, J9 Additional SPI Interface Signals

3.3 J10, J11 Third Serial Interface

Jumpers J10 and J11 are used to route the signals of the third synchronous/asynchronous serial interface via the RS-232 transceiver to the phyCORE connector pins X1C24 (RxD2) and X1C25 (TxD2). If the jumpers are closed in position 2+3, then the applicable controller pins PA21 and PA22 can be used with their alternative functions or the serial interface signals are available with their TTL level at phyCORE-connector pins X1C25 and X1C24.

If the jumpers are closed at position 1+2 we recommend **not** to use the interface signals with their TTL level as this will cause damage to the on-board components.

The following configurations are possible:

Signal Configuration	J10	J11
TxD2 and RxD2 with RS-232 levels	1 + 2*	1 + 2*
PA21 and PA22 as I/O pin or TxD2 and RxD2 as interface signals with TTL level	2 + 3	2 + 3

* = Default setting

Table 6: J10, J11 Third Serial Interface Configuration

3.4 J33 Reset Signal for Twin-CAN Controller 82C900

Jumper J33 is used to configure the Twin-CAN controller‘s reset signal and selects either port PB0 of the microcontroller or the module‘s /RESET line as CAN_RESET.

Note:
If jumper J33 remains closed at position 1+2, then port PB0 is used for the Twin-CAN controller reset signal. The Twin-CAN controller‘s reset input is important for the power-down features of the CAN controller, since it is only possible to exit the sleep mode of the 82C900 with a reset signal transition. *More information on the 82C900 power-down modes can be found in the Twin-CAN controller Data Sheet.*

The following configurations are possible:

Signal	J33
/RESET_CAN connected with module‘s /RESET line	2 + 3*
/RESET_CAN connected with PB0 of the microcontroller	1 + 2
No reset signal routed to the CAN controller (power-down mode can not be used)	open

* = Default setting

Table 7: J33 Reset Signal for CAN Controller Configuration

3.5 J12, J13 RAM Size Configuration

The phyCORE-AT91M55800A can be populated with three different RAM memory sizes per shape (U14 thru U17). The size of the device must be configured to ensure linear addressing of the entire RAM bank. Jumpers J12 and J13 are used to select the size of the memory device. The on-board CPLD reads the signal level on the applicable input pins and configures the individual Chip Select signals for the RAM devices accordingly.

Note:
Jumpers J12 and J13 are configured at time of delivery of the phyCORE-AT91M55800A according to the choosen memory configuration. Therefor these jumpers must **not** be altered by the user!

The following configurations are possible:

RAM Memory Size	J12	J13
512 kByte (per shape)	open*	open*
1 MByte (per shape)	closed	open
2 MByte (per shape)	open	closed
Not permitted	closed	closed

* = Default setting

Table 8: J12, J13 RAM Memory Size Configuration

3.6 J18, J19 Flash Size Configuration

The phyCORE-AT91M55800A can be populated with three different Flash memory sizes per shape (U6 thru U9). The size of the device must be configured to ensure linear addressing of the entire Flash bank. Jumpers J18 and J19 are used to select the size of the memory device. The on-board CPLD reads the signal level on the applicable input pins and configures the individual Chip Select signals for the Flash devices accordingly.

Note:
Jumpers J18 and J19 are configured at time of delivery of the phyCORE-AT91M55800A according to the choosen memory configuration. Therefor these jumpers must **not** be altered by the user!

The following configurations are possible:

Flash Memory Size	J18	J19
1 MByte (per shape)	open*	open*
2 MByte (per shape)	closed	open
4 MByte (per shape)	open	closed
Not permitted	closed	closed

* = Default setting

Table 9: J18, J19 Flash Memory Size Configuration

3.7 J14, J15, J16, J17 CAN Interfaces

The dual CAN interface of the phyCORE-AT91M55800A are provided by the Infineon 82C900 Twin-CAN controller. The Twin-CAN controller is connected to the AT91M55800A via the SPI interface. These CAN signals extend to the two CAN transceivers at U26 and U27 (PCA82C251, alternatively TLE6250). The CAN transceivers generate the corresponding CANH0, CANL0, CANH1 and CANL1 signals. These signals can be directly connected to a CAN dual-wire bus.

In order to use external (opto-isolated) transceivers, direct access to the CAN1Rx, CAN1Tx, CAN2Rx and CAN2Tx signals is also available at the phyCORE connector X1. This requires **both** removal of the CAN transceiver devices **and** closing Jumpers J14, J15, J16 and J17.

The following configurations are possible:

First CAN Interface	J14	J15
CAN_H0 at X1D21 CAN_L0 at X1D20	open*[1]	open*[1]
CAN0_Rx at X1D21 CAN0_Tx at X1D20	closed [2]	closed[2]

Second CAN Interface	J16	J17
CAN_H1 at X1C18 CAN_L1 at X1D18	open*[1]	open*[1]
CAN1_Rx at X1C18 CAN1_Tx at X1D18	closed[2]	closed[2]

* = Default setting

Table 10: J14, J15, J16 and J17 CAN Interface Configuration

[1] : Should only be used if CAN transceivers U26 and U27 are populated.

[2] : **Note!** Should only be used if CAN transceivers U26 and U27 are **NOT** populated.

3.8 J20, J21 A/D and D/A Converter

The integrated analog/digital and digital/analog converters on the phyCORE-AT91M55800A require an upper and lower reference voltage (V_{ADREF}, V_{DAVREF}) connected at pins 15 (D/A) and 45 (A/D). The reference voltage source can be selected using Jumpers J20 and J21.

The following configurations are possible:

Reference Voltage Configuration	J20	J21
external A/D reference voltage source (V_{ADVREF} at X1D50)		2 + 3*
V_{ADVREF} derived from main supply voltage VCC		1 + 2
external D/A reference voltage source (V_{DAVREF} at X1D42)	2 + 3*	
V_{DAVREF} derived from main supply voltage VCC	1 + 2	

* = Default setting

Table 11: J20, J21 A/D and D/A Converter Reference Voltage

3.9 J22 Back-up Reset Configuration

The integrated, battery buffered RTC on the AT91M55800A must be reset after being connected to the operating voltage (VPD or VCC depending on the configuration). The controller is equipped with a seperate backup reset input (RSTBU) for this purpose. There are two different reset sources available. With the help of Jumper J22 it is possible to select which of these sources is used.

For continual use of the RTC, even when the controller is in power-down mode, the RTC operating voltage must be derived from VPD. In order to be able to reset the RTC and its quartz oscillator the reset signal must be drawn from the RC time constant connected to VPD. In this configuration a reset signal is generated the first time the battery supply voltage is connected, thus guaranteeing successful start-up of the RTC quartz. With this configuration a continous event recording is possible, for example.

As an alternative, the reset input of the RTC unit can be connected to the signal generated by the reset controller at U5. In this case a restart of the RTC quartz and therefore of the entire RTC is generated following each falling edge of the reset signal.

The following configurations are possible:

Reset Signal for RTC	J22
Continous event recording	1 + 2*[1]
RTC restart following each /RESET	2 + 3

* = Default setting

Table 12: J22 RTC Reset Configuration

[1] : If J22 is closed at 1+2 the controller will only start after the module's reset input signal is toggled. This can be done by pressing and releasing the Reset push button on the phyCORE Development Board HD200. If an external battery is connected to the module (via VBAT at connector pin X1C6) this reset sequence is not required and the controller will start immediately after power-on.

3.10 J23, J35 CAN Transceiver Configuration

The phyCORE-AT91M55800A can be populated with three different CAN transceivers (U27 and U26), which vary in terms of the connection of pin 5. Pin 5 can be configured accordingly with Jumpers J23 and J35.

The following configurations are possible:

CAN Transceiver Supply	J23	J35
82C251, pin 5 open	open*	open*
TLE6250V33, pin 5 connected with VCC (3.3 V)	1 + 2	1 + 2
TLE6250V5, pin 5 connected with VCC2 (5 V)	2 + 3	2 + 3

* = Default setting

Table 13: J23, J35 CAN Transceiver Configuration

3.11 J24 Twin-CAN Controller Configuration

The 82C900 Twin-CAN controller (U28) can operate with either a 3.3 V or a 5 V supply voltage. Jumper J24 configures the supply voltage of the Twin-CAN controller.

Please refer to the CAN controller's data sheet for instructions on setting the supply voltage and operating the CAN controller with the various voltages.

The following configurations are possible:

Twin-CAN Controller Supply	J24
VCC2 (5 V) used as 82C900 supply voltage	1 + 2*
VCC (3.3 V) used as 82C900 supply voltage	2 + 3

* = Default setting

Table 14: J24 Twin-CAN Controller Configuration

3.12 J25 SRAM Supply Voltage

The SRAMs (U14-U17) can operate with or without a battery buffer. Jumper J25 is used to set the supply voltage for the SRAM.

The following configurations are possible:

SRAM U14-U17 Supply Voltage	J25
VCCRAM derived from VCC	1 + 2*
VCCRAM derived from VBAT	2 + 3

* = Default setting

Table 15: J25 SRAM Supply Voltage Configuration

3.13 J26, J28, J34 Ethernet Controller CS8900A Configuration

As an option, a CS8900A Ethernet controller from Cirrus Logic can populate the phyCORE-AT91M55800A at U23.

If the Ethernet controller CS8900A is populating the phyCORE module, one of three possible Chip Select signals for controlling access to the CS8900A can be selected using Jumper J28.

The Ethernet controller always starts in 8-bit mode following a reset. By toggling the /SBHE-pin the Ethernet controller can be switched into 16-bit mode. There are two possibilities for switching the operating mode of the Ethernet controller. With the help of Jumper J26 it is possible to select between these two options.

If Jumper J26 is closed at position 1+2, then the Ethernet controller will automatically switch to 16-bit mode when the corresponding CS-signal is accessed. If Jumper J26 is closed at position 2+3, then the /SBHE pin is connected with the address signal A0. This means that the access must occur on an uneven address of the CS8900A in order to switch the controller to 16-bit mode. If Jumper J26 remains open, then the Ethernet controller can only operate in 8-bit mode.

Jumper J34 selects, which of the microcontroller interrupts connects with the interrupt output of the Ethernet controller.

Note:
In order to operate the Ethernet controller in 16-bit mode, a DUMMY access to the CS8900A must occur initially. Depending on the configuration of J26, this initial access occurs via the applicable /CS signal or access to an odd memory address (A0 active). This DUMMY access causes a high pulse (L-H-L signal transition) on the /SBHE pin thus activating the 16-bit mode of the Ethernet controller. The DUMMY access has to occur following each Ethernet reset. *More information on the CS8900A operating modes can be found in the Ethernet controller Data Sheet.*

The following configurations are possible:

/CS Signal Configuration	J28
/CS2 from the µC selects Ethernet controller	1 + 2*
/CS3 from the µC selects Ethernet controller	2 + 4
/CS4 from the µC selects Ethernet controller	2 + 3

* = Default setting

Table 16: J28 Ethernet Chip Select Signal Configuration

Ethernet Mode	J26
16-bit mode, A0 controls /SBHE	2 + 3*
16-bit mode, /CS signal (*see J28*) controls /SBHE	1 + 2
8-bit mode	open

* = Default setting

Table 17: J26 Ethernet Mode Configuration

Interrupt of the Ethernet Controller...	J34
.. connects to /IRQ2 of the microcontroller	1 + 2*
.. connects to /IRQ3 of the microcontroller	2 + 4
.. connects to FIQ of the microcontroller	2 + 3

* = Default setting

Table 18: J34 Ethernet Interrupt Signal Configuration

3.14 J29, J30 Chip Select Configuration

If the phyCORE-AT91M55800A is delivered with the minimum memory configuration, then the CPLD device is not required. In this case Jumper J29 and J30 must be closed in order to connect the Chip Select signals for Flash and SRAM with the corresponding microcontroller signals. These jumpers remain open on all other memory configuration varaints of the phyCORE-AT91M55800A since the required Chip Select signals for Flash and SRAM must be decodede by the CPLD at U4 in order to ensure correct memory addressing.

The following configurations are possible:

Chip Select for Flash and RAM	J29	J30
Chip Selects for Flash and RAM decoded by the CPLD	open	open
Chip Selects for Flash and RAM directly connected to µC (/CS0 and /CS1)[1]	closed*	closed*

*** Note:**
If minimum configuration of the phyCORE-AT91M55800A is used these jumpers must be closed

Table 19: J29, J30 Chip Select Configuration

1: Only possible if minimum configuration of the phyCORE-AT91M55800A is used, CPLD not populated.

3.15 J31 Write Protection of EEPROM

Various types of EEPROM devices can populate space U29. Some of these devices provide a write protection function[1]. Closing Jumper J31 connects pin 3 of the serial EEPROM/FRAM with VCC and thus activates write protection.

The following configurations are possible:

Write Protection EEPROM	J31
Write protection of EEPROM deactivated	open*
Write protection of EEPROM activated	closed

* = Default setting

Table 20: J31 EEPROM Write Protection

3.16 J32 Supply Voltage for AT91M55800A I/O Pins

The I/O pins on the phyCORE-AT91M55800A can operate with either a 3.3 V or a 5 V supply voltage. Jumper J32 configures the appropriate supply voltage.

The following configurations are possible:

I/O Supply Voltage	J32
VDDIO connected with VCC (3.3 V)	1 + 2*
VDDIO connected with VCC2 (5 V)	2 + 3

* = Default setting

Table 21: J32 Supply Voltage for I/O Pins

1: *Refer to the corresponding EEPROM Data Sheet for more information on the write protection function.*

3.17 J36 CLKIN Configuration

Jumper J36 is used to input an external clock signal. In default settings the on-board quartz oscillator is used for generating the microcontroller's clock speed (Jumper J36 open). As an alternative an external clock signal can be connected to the controller pin XIN via phyCORE connector pin X1A1. This requires removal of the on-board quartz oscillator and closing J36.

Note:
Because of the oscillator properties, Jumper J36 cannot be closed when using the on-board quartz oscillator. This can have a negative effect on the stability of the quartz oscillation!
If an external clock input via X1A1 is required, the on-board quartz oscillator must be removed.

The following configurations are possible:

CLKIN Configuration	J36
Using the on-board crystal XT1	open*
Supply via external clock signal at phyCORE connector pin X1A1	closed

* = Default setting

Table 22: J36 CLKIN Configuration

3.18 J37 /WAIT Configuration

The AT91M55800A controller provides a /WAIT signal that supports control of external memory access. Whenever the /WAIT signal is active the controller automatically inserts wait state cycles for memory access. Closing Jumper J37 connects the controller's /WAIT signal with the Ready/Busy (RDY/BSY) signal on the Flash device. This allows very efficient timing and optimal access times whenever the controller performs write operations to the Flash. The controller will continue inserting wait state cycles as long as the /WAIT signal is in its active state.

Connecting the /WAIT signal with the RDY/BST signal on the Flash does not replace configuration of the corresponding EBI register.

The following configurations are possible:

/WAIT Configuration	J37
Flash Ready/Busy signal connected with controller's /WAIT input, configuration of EBI register still required	closed*
Wait state configuration in the EBI register of the corresponding /CS signal required	open[1]

* = Default setting

Table 23: J37 /WAIT Configuration

3.19 J38, J39 Second Serial Interface

Jumpers J38 and J39 are used to route the signals of the second synchronous/asynchronous serial interface via the RS-232 transceiver to the phyCORE connector pins X1C21 (RxD1) and X1C23 (TxD1). If the jumpers are closed in position 2+3, then the applicable controller pins PA18 and PA19 can be used with their alternative functions or the serial interface signals are available with their TTL level at phyCORE-connector pins X1C21 and X1C23.

If the jumpers are closed at position 1+2 we recommend **not** to use the interface signals with their TTL level as this will cause damage to the on-board components.

The following configurations are possible:

Signal Configuration	J38	J39
TxD1 and RxD1 with RS-232 levels	1 + 2*	1 + 2*
PA18 and PA19 as I/O pin or TxD1 and RxD1 as interface signals with TTL level	2 + 3	2 + 3

* = Default setting

Table 24: J38, J39 Second Serial Interface Configuration

[1]: If J37 remains open we recommend connecting the /WAIT signal via a pull-up resistor to VCC (3.3V) in order to ensure proper signal levels.

3.20 J27 /RESIN Configuration

Jumper J27 is used to configure the /RESIN signals. This configuration is necessary when populating the phyCORE-AT91M55800A with or without a CAN interface. If no CAN interface is populated, the Reset controller U2 is not populating the module. Jumper J27 must now be closed in order to direct the /RESIN signal to the Reset controller U5.

The following configurations are possible:

Signal Configuration	J27
/RESIN connected with Reset controller U5[1]	1 + 2*
/RESIN connected with Reset controller U2	2 + 3

* = Default setting

Table 25: J27 /RESIN Configuration

3.21 J40 SRAM Configuration

Jumper J40 is required for configuring the SRAM signals /LB and /UB. It configures the controller access to the various SRAM-types that can be populated on the phyCORE-AT91M55800A, since these can have various data bus configurations.

The following configurations are possible:

Signal Configuration	J40	J40
/LB and /UB signals configured for accessing fast SRAMs (i.e. 10 ns)	1 + 2*	3 + 4*
/LB and /UB signals configured for accessing standard SRAMs (i.e. 55 ns)	1 + 3	2 + 4

* = Default setting

Table 26: J40 SRAM Access Configuration

1: Only possible if Reset controller at U2 is not populated.

4 System Configuration

Following a hardware or software reset, the AT91M55800A microcontroller starts program execution from address 0000:0000H. At this address a jump instruction to an application-specific initialization routine is located. This routine configures certain features of the microcontroller. Initialization is carried out in a privileged mode. After that, access to specific registers and execution of certain instructions are limited.

Although most features of the AT91M55800A microcontroller are configured and/or programmed during the initialization routine, other features, which influence program execution, must be configured prior to initialization.

4.1 System Startup Configuration

The system startup configuration sets the features of the microcontroller that have a direct influence on program execution and, hence, the correct execution of the initialization routine as well.

During the system startup configuration, certain port pins are latched by the controller during the reset procedure. The signal level on the corresponding input pins configures the resulting characteristics of the controller. The system startup configuration can be set by connecting desired port pins with a pull-down resistor (resulting in logical 0), or by leaving the connections open (resulting in logical 1).

A 4.7 kΩ pull-down resistor is recommended, although the resistor value is also dependent upon the external circuitry that is connected to the data bus of the module.

Table 27 shows the functions of individual port pins during system start-up, the corresponding pull-down resistor and the location of the signals on the phyCORE connector:

Port Pin Functions during System Startup		
PB18 (X1B43)	PA18/TxD1//TRI (X1C21)	JTAGSEL (X1D37)
Boot Mode Select *R16* *populated*	/TRI *R17* *not switched against GND*	JTAGSEL *R18* *switched against GND*

Table 27: Functional Settings on Port Pins for System Startup Configuration

Default system start-up configuration on the phyCORE-AT91M55800A

The initial setting of the system startup configuration should be modified during the initialization routine (i.e. your startup code). Certain functions can not be configured during startup, such as selection of the number of wait states for individual memory devices and Chip Select signals, as well as the location of these devices within the controller's address space.

5 Memory Models

The AT91M55800A controller provides up to eight Chip Select signals for easy selection of external peripherals or memory banks. Depending on the number of memory devices installed on the phyCORE-AT91M55800A, as well as the availability of the optional Ethernet controller, up to three Chip Select signals are used internally. /CS0 selects the Flash bank installed on U6 - U9 with either 1 MByte, 2 MByte or 4 MByte devices in CBGA-48 packaging per shape. The total amount of Flash memory is 1 MByte in the minimum configuration of the module and 16 MByte if the maximum configuration is used.

The external data memory consists of the one RAM bank at U14 – U17. These spaces can house memory devices of 512 kByte, 1 MByte or 2 MByte in an TBGA-48 package. /CS1 selects the RAM bank on U14 – U17.

Access to the optional Ethernet controller at U23 can be established via /CS2, /CS3 or /CS4 configurable with Jumper J28. The default configuration allows access via /CS2 (J28 closed at 1+2).

The assignment of the Chip Select signals to specific address areas is done with the corresponding EBI_CSRx register. Ensure that the memory areas for the individual /CS signals do not overlap in order to avoid conflicts when accessing the desired code or data memory. Program code must remain accessible via /CS0.

Initially following a reset only /CS0 is active in a 1 MByte area of the controller's address space beginning at address 0x0000. This means that /CS0 enables access to Flash bank (U6-U9). The other /CS signals must first be activated via a remap command. This requires setting bit 0 in the corresponding EBI_RCR register. /CS0 is initially only active in this controller activated range.

If the physical memory is smaller than the configured memory size, the memory mirrors itself in the set address range depending on the populated memory device. This statement is only valid if the minimum configuration of the module is used (Jumper J30 closed). For all other configurations of the phyCORE-AT91M55800A with a CPLD device populating the module at U4 a different memory mapping scheme as shown below applies. The CPLD program configures various memory mirrors that allow easy testing of the memory devices.

Memory mapping example:

RAM_address is the RAM start address, for example: 0x4000000

If 512 kByte RAM devices are installed at U14-U17:

J12 = open, J13 = open

U14 mirrored 4 times from RAM_address + 0x800000 to RAM_address + 0x9FFFFF
(0x800000 - 0x87FFFF, 0x880000 - 0x8FFFFF, 0x900000 - 0x97FFFF,
0x980000 - 0x9FFFFF) 4* 512k in a row
U15 mirrored 4 times from RAM_address + 0xA00000 to RAM_address + 0xBFFFFF
U16 mirrored 4 times from RAM_address + 0xC00000 to RAM_address + 0xDFFFFF
U17 mirrored 4 times from RAM_address + 0xE00000 to RAM_address + 0xFFFFFF

If 1 MByte RAM devices are installed at U14-U17:

J12 = closed, J13 = open

U14 mirrored twice from RAM_address + 0x800000 to RAM_address + 0x9FFFFF
(0x800000 - 0x8FFFFF, 0x900000 - 0x9FFFFF) 2* 1M in a row
U15 mirrored twice from RAM_address + 0xA00000 to RAM_address + 0xBFFFFF
U16 mirrored twice from RAM_address + 0xC00000 to RAM_address + 0xDFFFFF
U17 mirrored twice from RAM_address + 0xE00000 to RAM_address + 0xFFFFFF

If 2 MByte RAM devices are installed at U14-U17:

J12 = open, J13 = closed

U14 mirrored once from RAM_address + 0x800000 to RAM_address + 0x9FFFFF
only single mirror
U15 mirrored once from RAM_address + 0xA00000 to RAM_address + 0xBFFFFF
U16 mirrored once from RAM_address + 0xC00000 to RAM_address + 0xDFFFFF
U17 mirrored once from RAM_address + 0xE00000 to RAM_address + 0xFFFFFF

If an address is accessed that has not been initialized, a "DATA ABORT" command is executed by the controller. The command then calls a corresponding software routine. If the command is not specified further, the controller will not carry out any additional instructions.

The EBI_CSRx registers are 32-bit in size and structured as follows:

Bit 31-20:	BA	Base Address
Bit 19-14:	not used	
Bit 13:	CSEN	Chip Select Enable bit
Bit 12:	BAT	Byte Access Type
Bit 11-9:	TDF	Data Float Output Time
Bit 8-7:	PAGES	Page Size
Bit 6:	not used	
Bit 5:	WSE	Wait State Enable Bit
Bit 4-2:	NWS	Number of Wait States
Bit 1-0:	DBW	Data Bus Width

Due to the internal structure of the AT91M55800A, the PLL factor of 2 and the external quartz frequency of 16 MHz, the controller operates at a bus cycle time of 31.25 ns (without any wait state settings). If a wait state is set, the bus cycle time increases by an entire clock cycle to 62.5 ns, however the /RD and /WE impulse only increases by half a clock cycle (15.675 ns). Only when setting a wait state value of >=2 the pulse times increase by 31.25 ns for each additional wait state.

By setting three wait states (Tc = 31.25 ns), all memory types can be addressed with access times of up to 100 ns with a bus cycle of 125 ns. In order to be able to operate the controller with a 32 MHz CPU clock speed without wait states, 15 ns memory devices must be populated. However, this also required use of the Early Read protocol[1].

With some peripheral devices it may be necessary to set "DATA FLOAT Times", since the devices are not able to release the data bus early.

[1]: *Further Information on the Early Read protocol are available in the AT91M55800A Data Sheet / User's Manual.*

The following paragraph contains important information on timing characteristics. All information refers to a AT91M55800A controller with a 16-bit bus at 32 MHz CPU clock time (F_{osz}).

Tc = 32.25 ns * Number of Wait States (NWS in EBI_CSRx)
Tf = 32.25 ns * Data Float Output Time (TDF in EBI_CSRx).

The following section contains two memory configuration examples for the phyCORE-AT91M55800A. These examples match the needs of most standard applications.

Example a)

EBI_CSR0:	010024A9h =	Range 0100:0000h – 013F:FFFFh (4 MByte Flash bank at U6-U9, 16-bit bus, 3 wait states, 2 cycle after transfer, byte write access, 90 ns memory access time)
EBI_CSR1:	040034A5h =	Range 0400:0000h – 043F:FFFFh (4 MByte RAM bank at U14-U17, 16-bit bus, 2 wait states, 2 cycle after transfer, byte select access, 70 ns memory access time)
EBI_CSR2:	2000342Dh =	Range 2000:0000h – 200F:FFFFh (1 MByte) address range for ext. Ethernet controller, 16-bit bus, 4 wait states, 2 cycle after transfer, access time 135 ns)
EBI_CSR3:	30000000h	/CS3 not active
EBI_CSR4:	40000000h	/CS4 not active
EBI_CSR5:	50000000h	/CS5 not active
EBI_CSR6:	60000000h	/CS6 not active
EBI_CSR7:	70000000h	/CS7 not active

Example b)

EBI_CSR0:	01002529h =	Range 0100:0000h – 01FF:FFFFh (16 MByte Flash bank at U6-U9, 16-bit bus, 3 wait states, 2 cycle after transfer, byte write access, 90 ns memory access time)
EBI_CSR1:	02003525h =	Range 0200:0000h – 02FF:FFFFh (16 MByte RAM bank at U14-U17, 16-bit bus, 2 wait states, 2 cycle after transfer, byte select access, 55 ns memory access time)
EBI_CSR2:	1000342Dh =	Range 1000:0000h – 100F:FFFFh (1 MByte) address range for ext. Ethernet controller, 16-bit bus, 4 wait states, byte select access, 2 cycle after transfer)
EBI_CSR3:	30000000h	/CS3 not active
EBI_CSR4:	40000000h	/CS4 not active
EBI_CSR5:	50000000h	/CS5 not active
EBI_CSR6:	60000000h	/CS6 not active
EBI_CSR7:	70000000h	/CS7 not active

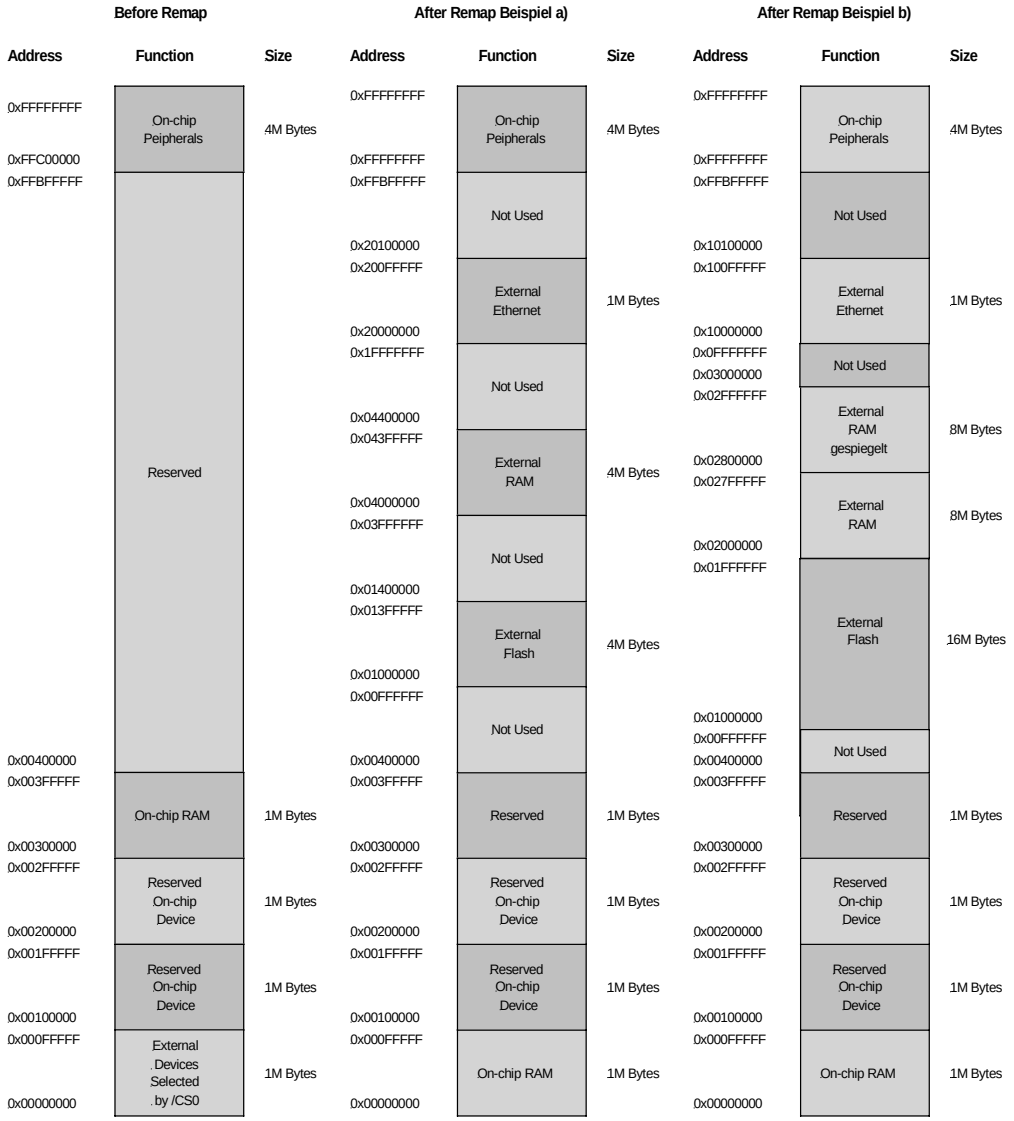


Figure 8: Memory Model Examples

6 Serial Interfaces

6.1 RS-232 Interfaces

One RS-232 transceiver is populating the phyCORE-AT91M55800A at U1. This device converts the signal levels for:

- PA16/RxD0 and PA15/TxD0 (frist serial interface)
- PA19/RxD1 and PA18/TxD1 (second serial interface)
- PA22/RxD2 and PA21/TxD2 (third serial interface).

The ports listed above can also be used alternatively as standard I/Os, as interface signals with TTL-level or in their alternative function on the phyCORE-connector X1. For this Jumpers J1 and J2 have to remain open, whereas J10 and J11 as well as J38 and J39 must be closed at position 2+3.

All RS-232 interfaces enable connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line is connected to the RxD line of the COM port. The Ground potential of the phyCORE-AT91M55800A circuitry needs to be connected to the applicable Ground pin on the COM port as well.

The microcontroller's on-chip UARTs do not support handshake signal communication. However, depending on user needs, handshake communication can be software emulated using port pins on the microcontroller. Use of an RS-232 signal level in support of hand-shake communication requires use of an external RS-232 transceiver not located on the module.

6.2 CAN Interface

The phyCORE-AT91M55800A is designed to house two CAN transceivers at U26 and U27 (either PCA82C251 or TLE6250). The CAN bus transceiver devices support signal conversion of the CAN transmit (CANTx) and receive (CANRx)lines. The CAN transceiver supports up to 110 nodes on a single CAN bus. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). In order to ensure proper message transmission via the CAN bus, a 120 Ohm termination resistor must be connected to each end of the CAN bus.

For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-AT91M55800A. This requires removal of the on-board CAN transceivers and routing the CANTx and CANRx lines to the phyCORE connector X1 by closing Jumpers J14, J15, J16 and J17. For connection of the CANTx and CANRx lines to an external transceiver we recommend using a Hewlett Packard HCPL06xx or a Toshiba TLP113 HCPL06xx fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

[1]: CiA: CAN in Automation. Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

7 Serial EEPROM (U29)

The phyCORE-AT91M55800A is populated with a non-volatile memory with a serial interface (SPI interface) to store configuration data. According to the memory configuration of the module an EEPROM (1 to 8 kByte) can be mounted at U29. *A description of the SPI protocol can be found in the applicable EEPROM Data Sheet.*

Table 28 gives an overview of the memory components that can be used at U29 at the time of printing of this manual.

Device Type	Size	Component	Manufacturer
EEPROM	1 kByte (1024*8)	AT25080	ATMEL
	2 kByte (2048*8)	AT25160	ATMEL
	4 kByte (4096*8)	AT25320	ATMEL
	8 kByte (8192*8)	AT25640	ATMEL

Table 28: Memory Device Options for U29

Various available EEPROM types provide a write protection function[1]. Jumper J31 is used to activate this function. If this jumper is closed, then pin 3 of the serial EEPROM is connected to GND. *Refer to section 3.15* for details on jumper settings for J31.

1: *Refer to the corresponding EEPROM Data Sheet for more information on the write protection function.*

8 On-Board Flash Memory (U6-U9)

Use of Flash as non-volatile memory on the phyCORE-AT91M55800A provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCORE-AT91M55800A:

- 29LV800B with 1*16 kByte, 2*8 kByte, 1*32 kByte, 15*64 kByte
- 29LV160B with 1*16 kByte, 2*8 kByte, 1*32 kByte, 31*64 kByte
- 29LV320B with 8*8 kByte, 63*64 kByte

These Flash devices are programmable with 3.3 V. No dedicated programming voltage is required.

Use of a Flash device as the only code memory results in no or only a limited usability of the Flash memory as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash-internal programming process, the reading of data from Flash is not possible. Hence, for Flash programming, program execution must be transferred out of Flash (such as into von Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

If the phyCORE-AT91M55800A is populated with multiple Flash devices on the available Flash bank it is possible to store application data in a Flash area which is physically seperated from the Flash area that contains program code.

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

9 CS8900A Ethernet Controller

Connection of the phyCORE-AT91M55800A to the world wide web or a local network is possible if the optional CS8900A 10-Mbit Ethernet Controller populates the module at U23.

This section only describes the functional characteristics of the CS8900A as implemented on the phyCORE-AT91M55800A. A detailed description of the Ethernet controller itself can be found in the corresponding datasheet for the Crystal LAN Ethernet controller from Cirrus Logic.

9.1 Operational Modes

Crystal LAN CS8900A Ethernet controller from Cirrus Logic offers various operational modes. The following sections explain the I/O mode and the memory mode of the Ethernet controller.

9.1.1 I/O Mode

The I/O mode is enabled following a reset of the module. This I/O mode allows the user to configure and operate the Ethernet controller within a lower address range of the microcontroller. In this mode the internal memory area of the CS8900A can be accessed via 2 registers, the "PackagePage-Pointer" and the "PackagePage-Data" registers. These registers possess the following default base addresses within the Ethernet controller‘s address space:

PackagePage-Pointer (default) : 0x30A
PackagePage-Data (default) : 0x30C

The PackagePage base address can be modified in the IO BASE REGISTER of the Ethernet controller.

9.1.2 Memory Mode

Following a reset of the module the memory mode of the CS8900A is not enabled. In order to render the Ethernet controller into memory mode an access via the address/data bus to the BUS CONTROL register (address = PackagPage base + 0x116, MemoryE = 1) must take place.

Once this sequence is completed, the entire internal 4 kByte address space of the CS8900A is available for read and write access. The base address in memory mode is set to 0x00 as default. However, this base address can be modified by configuration of the MEMORY BASE ADRESS register. The memory mode allows for faster operation of the Ethernet controller, in contrast to the I/O mode, due to the direct memory access.

Address range memory mode (default): 0x0000 – 0x0FFF

9.2 8-/16-bit Mode

The Ethernet controller is operated in 16-bit mode on the standard version of the phyCORE-AT91M55800A. Since the CS8900A starts in 8-bit mode after reset an access via the address/data bus must take place to switch into 16-bit mode before further configuration can be done. Jumper J26 (*refer to section 3.13*) configures how the Ethernet controller is switched into 16-bit mode. This switching can be accomplished by simple access to the device (via Chip-Select) or by access to an odd address (via A0) within the address space of the CS8900A.

9.3 Addressing the Ethernet Controllers

Various configuration options for Jumpers J26, J28 and J34 are available for select addressing of the Ethernet controller (*refer to section 3.13*). The CS8900A can be addressed via the configured Chip-Select signal.

In addition, the timing parameters, the controller base address within the address space as well as the operational mode must be considered when accessing the Ethernet controller.

When operating the Ethernet controller with access times of about 135 ns and with an Atmel AT91M55800A controller bus cycle time of 31.75 ns it is necessary to configure at least 5 wait states in the microcontroller‘s CSR registers to ensure correct operation.

Activation of the "Early Read" protocol is not recommended due to the accomplished slow access times. Definition of the Ethernet controller base address in the EBI_CSR register completes addressing configuration for the CS8900A.

Example for bus configuration using the EBI_CSR registers:

EBI_CSR 2 = 0x02002431	:	16-bit bus width, 5 wait states, wait states enable, 1 MB page, 2 TDF’s, CS enable, byte select access type, base address 0x2000000

9.4 Interrupt

The CS8900A Ethernet controller provides 4 interrupt outputs that are connected to each other on the phyCORE-AT91M55800A. This is possible since only one of the interrupt outputs is active at a given time while the other three outputs remain in tri-state mode.

Jumper J34 on the phyCORE-AT91M55800A (*refer to section 3.13 for detailed description*) must be configured to route the interrupt output to the corresponding input on the AT91M55800A, thus enabling interrupt-driven operation of the Ethernet controller.

With correct configuration it is possible to start an interrupt service routine on the Atmel AT91M55800A after the CS8900A Ethernet controller has received an Ethernet frame.

9.5 Hardware Standby

The CS8900A Crystal LAN Ethernet controller offers a hardware power-down mode for applications requiring power-saving options. The /SLEEP input signal of the Ethernet controller must be set to low level in order to activate the power-down mode. The /SLEEP signal is connected with the AT91M55800A controller‘s /SHDN line on the phyCORE module.

9.6 MAC Address

The MAC (Media Access Control) address is a **unique** identification code of computer hardware operating within a LAN (Local Area Network). When connecting the hardware to the Internet the assigned IP number is mapped to the MAC address via a conversion table.

The MAC addresses are administered in a central location in order to ensure the uniqueness of these numbers. PHYTEC has purchased a pool of such MAC addresses and each one of our Ethernet-based Single Board Computers gets one of these addresses.

The MAC address of your phyCORE-AT91M55800A is printed on a barcode sticker attached to the module. The MAC address is provided as a 12-digit hexadecimal value. In addition, the MAC address is also programmed into the Ethernet controller EEPROM (U22) at the time of delivery. This allows immediate start-up of the module and its Ethernet hardware. Following a hardware-reset the MAC address is automatically loaded from the EEPROM into the Ethernet controller (*refer to section 9.7*).

9.7 Ethernet EEPROM (U22)

The EEPROM connected to the Ethernet controller can be used to store specific confguration data that are automatically loaded into the CS8900A following a hardware-reset. The EEPROM can be programmed on-board via the Ethernet controller. Please refer to the Crystal LAN CS8900A Ethernet controller datasheet for details.

The MAC address is pre-programmed into the EEPROM (U22) at time of delivery (*refer to section 9.6*).

9.8 10Base-T Interface

The phyCORE-AT91M55800 has been designed exclusively for operation in 10Base-T networks. The 10Base-T interface with its signals LANLED and LINKLED extends to phyCORE-connector X1. The AUI interface of the CS8900A is not available on the connector.

Additional external circuitry is required to connect the module to an existing 10Base-T network. It should be noted that the 3 V version of the CS8900A controller (CS8900A-Q3) is used on the phyCORE-AT91M55800. Please refer to the Crystal LAN CS8900A Ethernet controller datasheet for details on the external circuitry design. This circuitry is also available from PHYTEC on a Ethernet adapter module, order code EAD-001 (*refer to section 15*).

10 Battery Buffer

The connection of a battery buffer is not essential to the functioning of the phyCORE-AT91M55800A. However, this battery buffer embodies an economical and practical means of storing data in the SRAM devices. It is necessary to preserve data from the on-chip Real-Time Clock of the AT91M55800A in case of a power failure.

The VBAT input at pin X1C6 of the board is provided for connecting the external battery. The negative polarity pin on the battery must be connected to GND on the phyCORE-AT91M55800A. As of the printing of this manual, a lithium battery is recommended as it offers relatively high capacity at low discharge. In the event of a power failure at VCC, the RTC will be buffered by a connected battery via VBAT. The RTC is generally supplied via VPD in order to preserve data by means of the battery back-up in the absence of a power supply via VCC.

The battery supply for the SRAM devices is configured with Jumper J25 *(refer to section 3.12)*. If the SRAM battery supply is enabled the user must ensure that the battery is capable of supplying both SRAM and RTC at runtime of the module.

Power consumption depends on the installed components and memory size (*see section 12, "Technical Specifications"*).

11 Debug Interface

The phyCORE-AT91M55800A is equipped with a JTAG interface for downloading program code into the external Flash or for debugging programs in the external SRAM. The JTAG interface extends out to 2 mm pitch pin header rows X2 on the controller side of the module. *Figure 9* and *Figure 10* show the position of the debug interface (JTAG connector X2) on the phyCORE module.

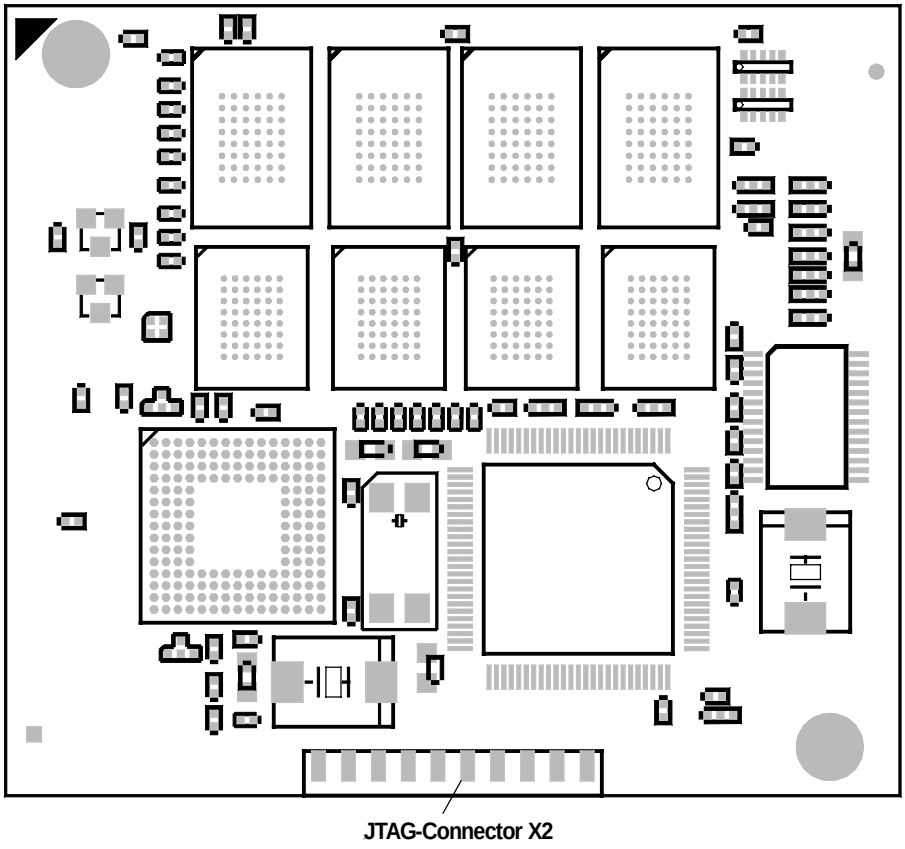


Figure 9: JTAG Interface (Top View)

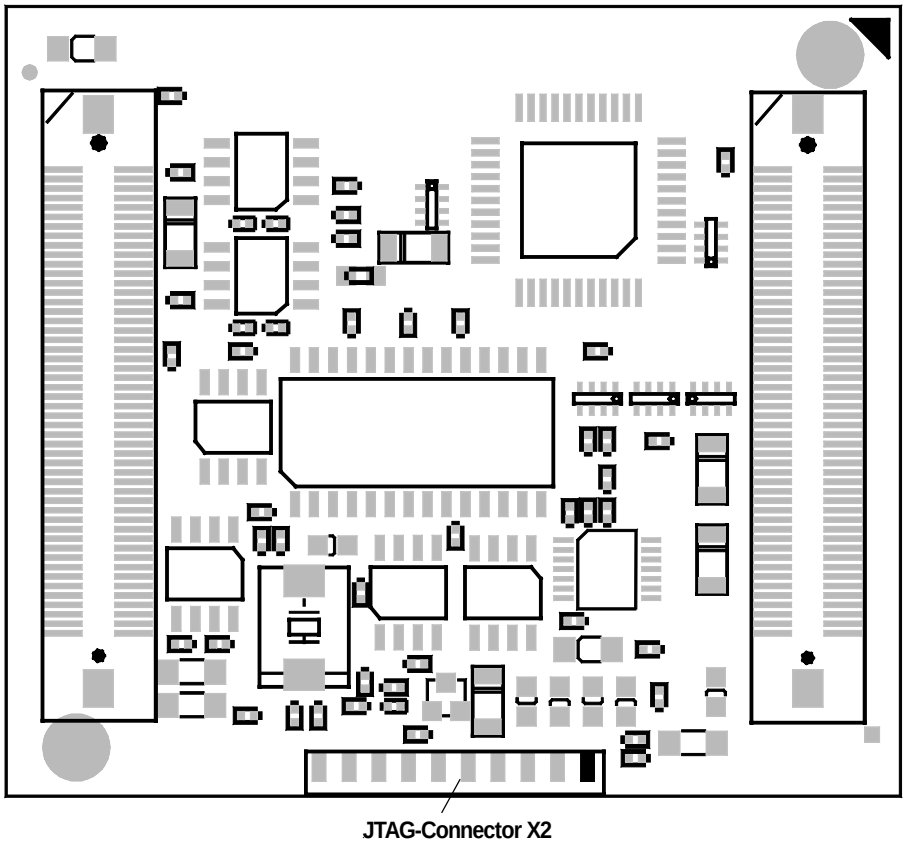


Figure 10: JTAG Interface (Bottom View)

Pin 1 of the JTAG concector X2 is marked by a black pad on the connector side of the PCB.

The JTAG interface of the phyCORE-AT91M55800A can operate in various modes. The signals /BSCAN and /JTAGSEL available on the pin header row X2 are responsible for switching between modes.

The following configuration options are available:

/BSCAN	/JTAGMODE	JTAG Interface Function
1	1	JTAG ICE debug mode
0	1	Boundary-Scan mode for programming the PLD controller in tri-state
1	0	Boundary-Scan mode of the AT91M55800A controller
0	0	not allowed

Table 29: JTAG Modes

Note:
The JTAG connector X2 only populates phyCORE-AT91M55800A modules with order code PCM-014-D. This version of the phyCORE module is included in all Rapid Development Kits (order code KPCM-014). JTAG connector X2 is not populated on phyCORE modules with order code PCM-014 that are intended for OEM implementation. However, all JTAG signals are also accessible at the phyCORE-connector X1 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See Table 56 for details on the JTAG signal pin assignment.*

PHYTEC offes a JTAG-Emulator adapter (order code JA-002) for connecting the phyCORE-AT91M55800A to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2.54 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X2 to standard Emulator connectors.

12 Technical Specifications

The physical dimensions of the phyCORE-AT91M55800A are represented in *Figure 11*. The module's profile is ca. 7.2 mm thick, with a maximum component height of 2.6 mm on the bottom (connector) side of the PCB and approximately 3.0 mm on the top (microcontroller) side. The board itself is approximately 1.6 mm thick.

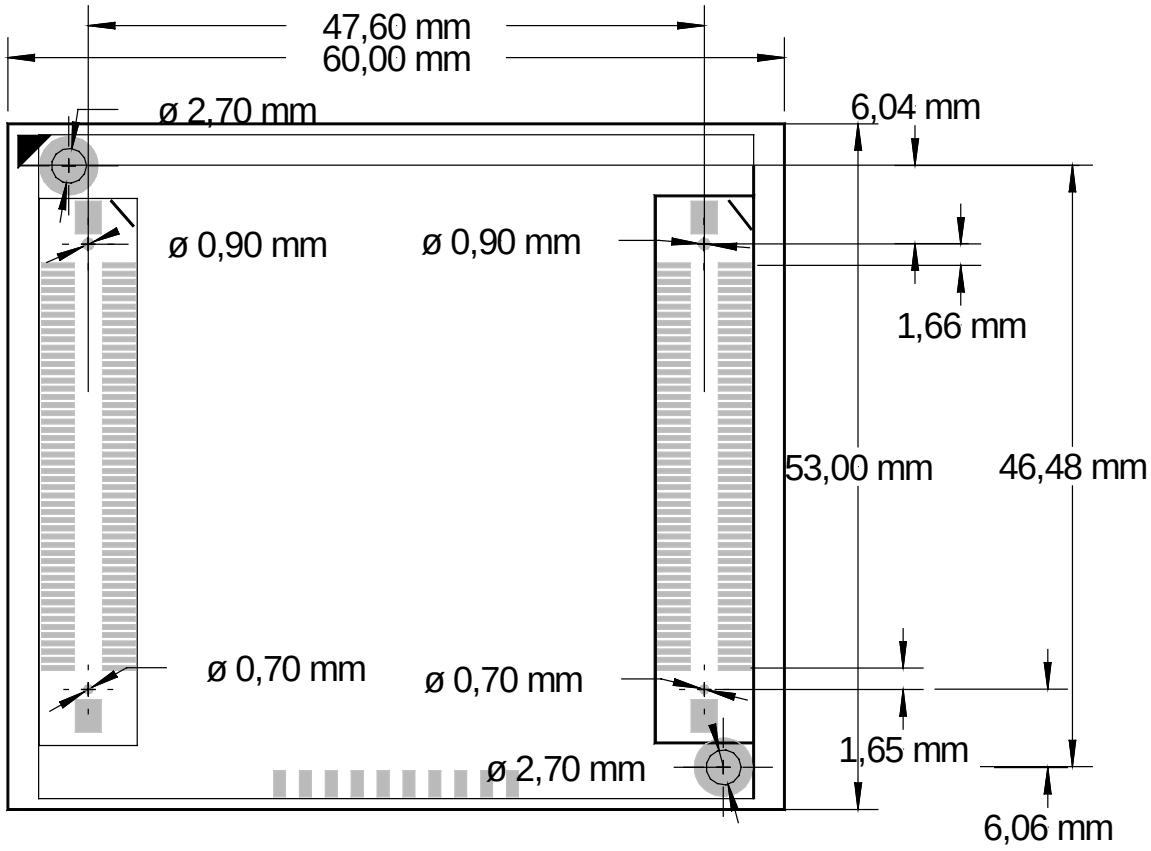


Figure 11: Physical Dimensions

Additional specifications:

• Dimensions:	60 mm x 53 mm
• Weight:	approximately 25 g with all optional components mounted on the circuit board
• Storage temperature:	-40°C to +90°C
• Operating temperature:	standard: 0°C to +70°C extended: -40°C to +85°C
• Humidity:	95 % r.F. not condensed
• Operating voltage:	VCC 3.3 V 5 %, VCC2 5 V 5 %, VBAT 3 V 20 %
• Power consumption: maximum 220 mA typical 110 mA	Conditions: **VCC = 3.3 V, VBAT = 0 V**, 512 kByte RAM, 1 MByte Flash, 16 MHz quartz, 20°C

These specifications describe the standard configuration of the phyCORE-AT91M55800A as of the printing of this manual.

Please note that the module storage temperature is only 0°C to +70°C if a battery buffer is used for the RAM devices.

13 Hints for Handling the phyCORE-AT91M55800A

The address and data bus on the module is not buffered. To connect external components to the data/address bus, as well as the control lines (/RD, /WR), an external buffer (i.e. 74AHCT245) between the modul and the peripheral components should be installed.

The data bus D0…15 (Port 0) should be connected with a 100 kΩ pull-up resistor against VCC.

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

14 The phyCORE-AT91M55800A on the phyCORE Development Board HD200

PHYTEC Development Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Development Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in labratory environments prior to their use in customer designed applications.

14.1 Concept of the phyCORE Development Board HD200

The phyCORE Development Board HD200 provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-AT91M55800A Single Board Computer module. The Development Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.
This modular development platform concept is depicted in *Figure 12* and includes the following components:

- The actual **Development Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **serial interfaces** (3) of the SBC module at DB-9 connectors (depending on the module, up to two RS-232 interfaces and up to two RS-485 or CAN interfaces).
- All of the signals from the SBC module mounted on the Development Board extend to two mating receptacle connectors. A strict 1:1 signal assignment is consequently maintained from the phyCORE-connectors on the module to these expansion connectors. Accordingly, the pin assignment of the **expansion bus** (4) depends entirely on the pinout of the SBC module mounted on the Development Board.

- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Development Boards, we are able to offer various **expansion boards** (5) that attach to the Development Board at the expansion bus connectors. These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Development Board.
- All controller and on-board signals provided by the SBC module mounted on the Development Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Development Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 12 illustrates the modular development platform concept:

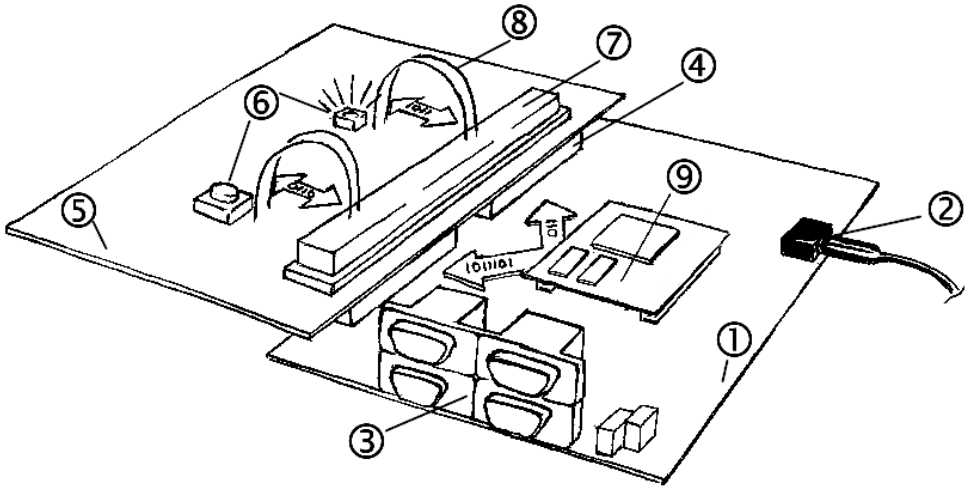


Figure 12: Modular Development and Expansion Board Concept with the phyCORE-AT91M55800A

The following sections contain specific information relevant to the operation of the phyCORE-AT91M55800A mounted on the phyCORE Development Board HD200. For a general description of the Development Board, please refer to the corresponding Development Board Hardware Manual.

14.2 Development Board HD200 Connectors and Jumpers

14.2.1 Connectors

As shown in *Figure 13*, the following connectors are available on the phyCORE Development Board HD200:

X1- low-voltage socket for power supply connectivity
X2- mating receptacle for expansion board connectivity
P1- dual DB-9 sockets for serial RS-232 interface connectivity
P2- dual DB-9 connectors for CAN or RS-485 interface connectivity
X4- voltage supply for external devices and subassemblies
X5- GND connector (for connection of GND signal of measuring devices such as an oscilliscope)
X6- phyCORE-connector enabling mounting of applicable phyCORE modules
X7- interface for Ethernet transformer module EAD-001
U9/U10- space for an optional silicon serial number chip
BAT1- receptacle for an optional battery

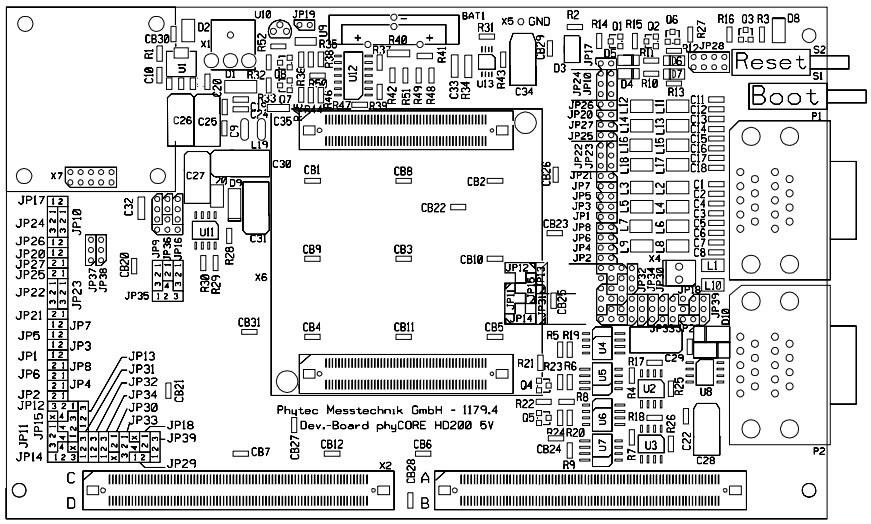


Figure 13: Location of Connectors on the phyCORE Development Board HD200

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

14.2.2 Jumpers on the phyCORE Development Board HD200

Peripheral components of the phyCORE Development Board HD200 can be connected to the signals of the phyCORE-AT91M55800A by setting the applicable jumpers.

The Development Board's peripheral components are configured for use with the phyCORE-AT91M55800A by means of insertable jumpers. If no jumpers are set, no signals connect to the DB-9 connectors, the control and display units and the CAN transceivers. The Reset input on the phyCORE-AT91M55800A directly connects to the Reset button (S2). *Figure 14* illustrates the numbering of the jumper pads, while *Figure 15* indicates the location of the jumpers on the Development Board.

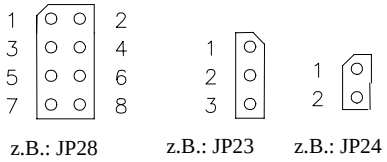


Figure 14: Numbering of Jumper Pads

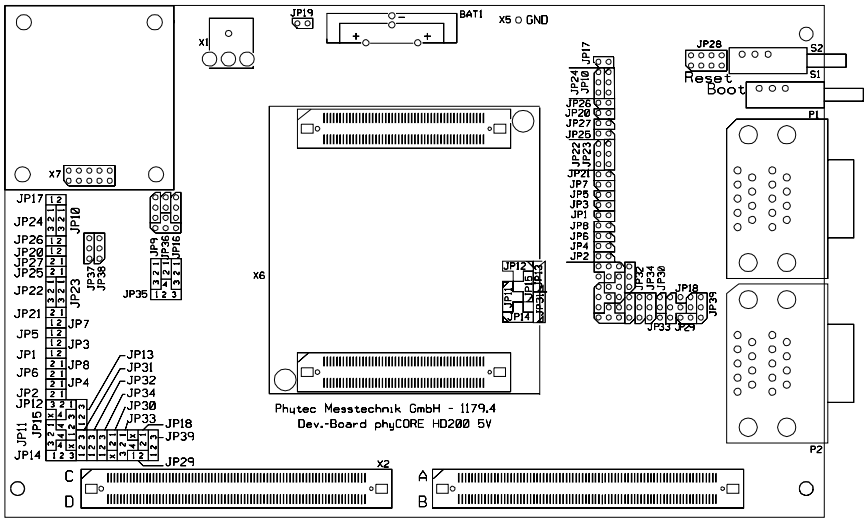


Figure 15: Location of the Jumpers (View of the Component Side)

Figure 16 shows the factory default jumper settings for operation of the phyCORE Development Board HD200 with the standard phyCORE-AT91M55800A (standard = AT91M55800A controller, use of first and second RS-232 interfaces and LED D3 on the Development Board). Jumper settings for other functional configurations of the phyCORE-AT91M55800A module mounted on the Development Board are described in *section 14.3*.

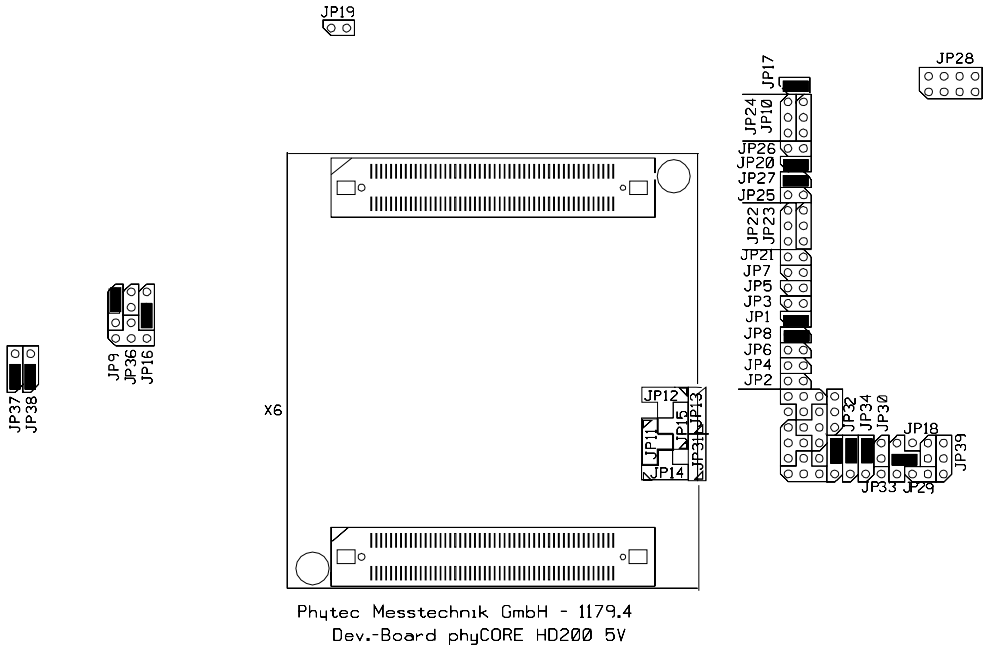


Figure 16: Default Jumper Settings of the phyCORE Development Board HD200 with phyCORE-AT91M55800A

14.2.3 Unsupported Features and Improper Jumper Settings

The following table contains improper jumper settings for operation of the phyCORE-AT91M55800A on a phyCORE Development Board HD200. Functions configured by these settings are not supported by the phyCORE module.

No RS-485 interface:

DB-9 plug P2B on the Development Board can be configured as RS-485 interface as an alternative to the second CAN interface. The phyCORE-AT91M55800A does not support an RS-485 interface. For this reason the corresponding jumper settings should never be used.

Jumper	Setting	Description
JP30	closed	TxD signal for second serial interface routed to pin 8 on the DB-9 plug P2B
JP33	1 + 2	RxD signal for second serial interface routed to pin 2 on the DB-9 plug P2B

Table 30: Improper Jumper Setting for JP30/33 on the Development Board

Reference Voltage Source for A/D Converter

Pins X1C42, X1C47, X1D39, X1D44 and X1D49 (VAGND) of the phyCORE-AT91M55800A are solely connected with the phyCORE Development Board HD200 GND potential. This makes a separate supply with an alternative VAGND potential impossible. Free definition of the VAGND potential is however available in a customer application board.

14.3 Functional Components on the phyCORE Development Board HD200

This section describes the functional components of the phyCORE Development Board HD200 supported by the phyCORE-AT91M55800A and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-AT91M55800A module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in *Figure 16* and enable alternative or additional functions on the phyCORE Development Board HD200 depending on user needs.

14.3.1 Power Supply at X1

Caution:
Do not use a laboratory adapter to supply power to the Development Board! Power spikes during power-on could destroy the phyCORE module mounted on the Development Board! Do not change modules or jumper settings while the Development Board is supplied with power!

Permissible input voltage: +/-5 VDC regulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-AT91M55800A mounted on the Development Board as well as whether an optional expansion board is connected to the Development Board. An adapter with a minimum supply of 500 mA is recommended.

Jumper	Setting	Description
JP9	1 + 2	3.3 V primary main supply voltage to the phyCORE-AT91M55800A
JP16	2 + 3	5 V as secondary main supply voltage to the phyCORE-AT91M55800A

Table 31: JP9, JP16 Configuration of the Main Supply Voltages VCC / VCC2

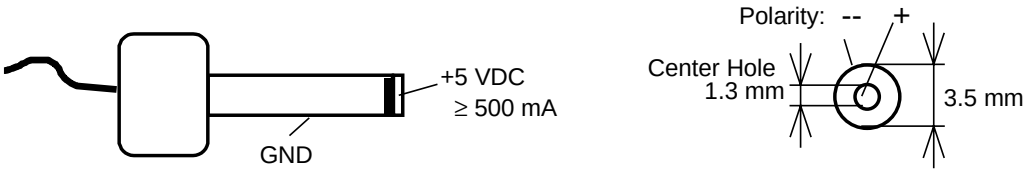


Figure 17: Connecting the Supply Voltage at X1

Caution:
When using this function, the following jumper settings are not allowed:

Jumper	Setting	Description
JP9	2 + 3	5 V as primary main supply voltage for the phyCORE-AT91M55800A
	open	phyCORE-AT91M55800A not connected to primary main supply voltage
JP16	1 + 2	3.3 V as secondary main supply voltage for the phyCORE-AT91M55800A
	open	phyCORE-AT91M55800A not connected to secondary main supply voltage **NOTE: This setting is correct if the module in its minimum configuration without CAN is used.**

Table 32: JP9, JP16 Improper Jumper Settings for the Main Supply Voltages

Setting Jumper JP9 to position 2+3 configures a primary main power supply to the phyCORE-AT91M55800A of 5 V which could destroy the module. Setting Jumper JP16 to position 1+2 configures a secondary main power supply to the phyCORE-AT91M55800A of 3.3 V which also can damage the module. If Jumper JP9 and JP16 remain open, no primary and secondary main power supply is connected to the phyCORE-AT91M55800A. These jumper settings should therefore not be used.

14.3.2 First Serial Interface at Socket P1A

Socket P1A is the lower socket of the double DB-9 connector at P1. P1A is connected via jumpers to the first serial interface of the phyCORE-AT91M55800A.

Jumper	Setting	Description
JP20	closed	Pin 2 of DB-9 socket P1A connected with RS-232 signal TxD0 of the phyCORE-AT91M55800A
JP21	open	Pin 9 of DB-9 socket P1A not connected
JP22	open	Pin 7 of DB-9 socket P1A not connected
JP23	open	Pin 4 of DB-9 socket P1A not connected
JP24	open	Pin 6 of DB-9 socket P1A not connected
JP25	open	Pin 8 of DB-9 socket P1A not connected
JP26	open	Pin 1 of DB-9 socket P1A not connected
JP27	closed	Pin 3 of DB-9 socket P1A connected with RS-232 signal RxD0 from the phyCORE-AT91M55800A

Table 33: Jumper Configuration for the First RS-232 Interface

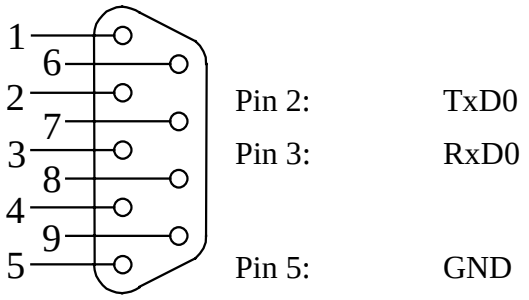


Figure 18: Pin Assignment of the DB-9 Socket P1A as First RS-232 (Front View)

Caution:

When using the DB-9 socket P1A as RS-232 interface on the phyCORE-AT91M55800A the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP20	open	Pin 2 of DB-9 socket P1A not connected, no connection to TxD0 signal from phyCORE-AT91M55800A
JP21	closed	Pin 9 of DB-9 socket P1A connected with port PB0 from phyCORE-AT91M55800A
JP22	1 + 2	Pin 7 of DB-9 socket P1A connected with port PA27 (/PCS1) from phyCORE-AT91M55800A
JP23	1 + 2	Pin 4 of DB-9 socket P1A connected with port PA24 (MISO) from phyCORE-AT91M55800A
JP24	1 + 2	Pin 6 of DB-9 socket P1A connected with port PA23 (SPCK) from phyCORE-AT91M55800A
	2 + 3	Pin 6 of DB-9 socket P1A connected with VOUT from Development Board HD200
JP25	Closed	Pin 8 of DB-9 socket P1A connected with port PA20 (SCK2) from phyCORE-AT91M55800A
JP26	closed	Pin 1 of DB-9 socket P1A connected with port PB2 from phyCORE-AT91M55800A
JP27	open	Pin 3 of DB-9 socket P1A not connected, no connection to RxD0 signal from phyCORE-AT91M55800A

Table 34: Improper Jumper Settings for DB-9 Socket P1A as First RS-232

If an RS-232 cable is connected to P1A, the voltage level on the RS-232 lines could destroy the phyCORE-AT91M55800A.

14.3.3 Power Supply to External Devices via Socket P1A

The phyCORE Development Board HD200 can be populated by additional components that provide a supply voltage of 5 V at pin 6 of DB-9 socket P1A. This allows for easy and secure supply of external devices connected to P1A. This power supply option especially supports connectivity to analog and digital modems. Such modem devices enable global communication of the phyCORE-AT91M55800A over the Internet or a direct dial connection.

The following figure shows the location of these components on the Development Board:

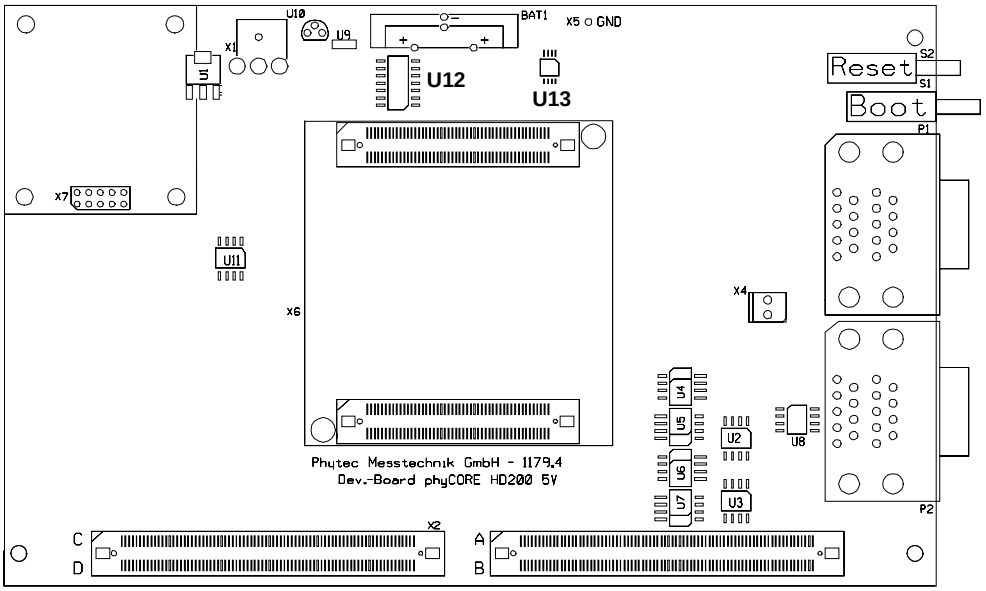


Figure 19: Location of Components at U12 and U13 for Power Supply to External Subassemblies

The components at U12 and U13 guarantee electronic protection against overvoltage and excessive current draw at pin 6 of P1A; in particular:

- Load detection and controlled voltage supply switch-on:

  In order to ensure clear detection of the switch-on condition, the connected device should cause a current draw of at least 10 mA at pin 6. The controlled voltage supply switch-on prevents voltage drop off on the phyCORE Development Board HD200.

- Overvoltage Protection:

  If the voltage at pin 6 exceeds the limiting value that can be provided by the phyCORE Development Board HD200, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board HD200 as well as connected modules and expansion boards.

- Overload Protection:

  If the current draw at pin 6 exceeds the limiting value of approximately 150 mA, the voltage at pin 6 will be switched off immediately. This prevents damage to the phyCORE Development Board HD200 and its power adapter caused by current overload.

This configuration option provides the following possibility:

Jumper	Setting	Description
JP24	2 + 3	Electronically protected 5 V at pin 6 for supply of external devices connected to P1A

Table 35: JP24 Power Supply to External Devices Connected to P1A on the Development Board

14.3.4 Second Serial Interface at Socket P1B

Socket P1B is the upper socket of the double DB-9 connector at P1. P1B is connected via jumpers to the second serial interface of the phyCORE-AT91M55800A. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the second serial interface (*refer to section 3.19*).

Jumper	Setting	Description
JP1	closed	Pin 2 of DB-9 socket P1B connected with RS-232 signal TxD1_RS232[1] of the phyCORE-AT91M55800A
JP2	open	Pin 9 of DB-9 socket P1B not connected
JP3	open	Pin 7 of DB-9 socket P1B not connected
JP4	open	Pin 4 of DB-9 socket P1B not connected
JP5	open	Pin 6 of DB-9 socket P1B not connected
JP6	open	Pin 8 of DB-9 socket P1B not connected
JP7	open	Pin 1 of DB-9 socket P1B not connected
JP8	closed	Pin 3 of DB-9 socket P1B connected with RS-232 signal RxD1_RS232[2] of the phyCORE-AT91M55800A

Table 36: Jumper Configuration of the DB-9 Socket P1B (Second RS-232)

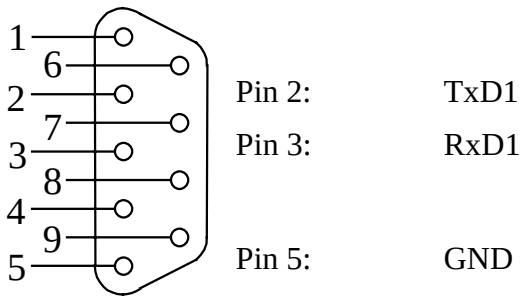


Figure 20: Pin Assignment of the DB-9 Socket P1B as Second RS-232 (Front View)

[1] : Check configuration of Jumper J39 on the phyCORE-AT91M55800A, *refer to section 3.19.*

[2] : Check configuration of Jumper J38 on the phyCORE-AT91M55800A, *refer to section 3.19.*

Caution:

When using the DB-9 socket P1B with the configuration of the phyCORE-AT91M55800A as described above the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP1	open	Pin 2 of DB-9 socket P1B not connected, no connection to TxD1 signal from phyCORE-AT91M55800A
JP2	closed	Pin 9 of DB-9 socket P1B connected with port PA28 (/PCS2) from phyCORE-AT91M55800A
JP3	closed	Pin 7 of DB-9 socket P1B connected with port TxD2_RS232 from phyCORE-AT91M55800A
JP4	closed	Pin 4 of DB-9 socket P1B connected with port PA26 (/PCS0) from phyCORE-AT91M55800A
JP5	closed	Pin 6 of DB-9 socket P1B connected with port PA25 (MOSI) from phyCORE-AT91M55800A
JP6	closed	Pin 8 of DB-9 socket P1B connected with port RxD2_RS232 from phyCORE-AT91M55800A
JP7	closed	Pin 1 of DB-9 socket P1B connected with port PA29 (/PCS3) from phyCORE-AT91M55800A
JP8	open	Pin 3 of DB-9 socket P1B not connected, no connection to RxD1 signal from phyCORE-AT91M55800A

Table 37: Improper Jumper Settings for DB-9 Socket P1B (Second RS-232)

If an RS-232 cable is connected to P1B by mistake, the voltage level on the RS-232 lines could destroy the phyCORE-AT91M55800A.

14.3.5 Third Serial Interface at Socket P1B

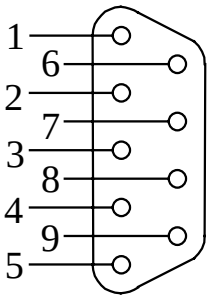
Socket P1B is the upper socket of the double DB-9 connector at P1. P1B can be connected, as an alternative to the second serial interface (*refer to section 14.3.4*), via jumpers to the third serial interface of the phyCORE-AT91M55800A. The following description is based on a module configuration that utilizes the on-board RS-232 transceivers for the second serial interface (*refer to section 3.3*).

Note:
In order to be able to use all three serial interfaces of the phyCORE-AT91M55800A on both of the Development Board's DB-9 sockets P1A and P1B, it is possible to connect socket P1B with the signals from the second and third serial interface **at the same time**. Please be aware of the non-standard DB-9 pin assignment in this case!

Jumper	Setting	Description
JP1	open	Pin 2 of DB-9 socket P1B not connected
JP2	open	Pin 9 of DB-9 socket P1B not connected
JP3	closed	Pin 7 of DB-9 socket P1B connected with RS-232 signal TxD2_RS232[1] of the phyCORE-AT91M55800A
JP4	open	Pin 4 of DB-9 socket P1B not connected
JP5	open	Pin 6 of DB-9 socket P1B not connected
JP6	closed	Pin 8 of DB-9 socket P1B connected with RS-232 signal RxD2_RS232[2] of the phyCORE-AT91M55800A
JP7	open	Pin 1 of DB-9 socket P1B not connected
JP8	open	Pin 3 of DB-9 socket P1B not connected

Table 38: Jumper Configuration of the DB-9 Socket P1B (Third RS-232)

[1] : Check configuration of Jumper J10 on the phyCORE-AT91M55800A, *refer to section 3.3*.
[2] : Check configuration of Jumper J11 on the phyCORE-AT91M55800A, *refer to section 3.3*.



Pin 2: TxD1[1]
Pin 7: TxD2
Pin 3: RxD1[1]
Pin 8: RxD2
Pin 5: GND

Figure 21: Pin Assignment of the DB-9 Socket P1B as 3rd RS-232 (Front View[2])

Caution:
When using the DB-9 socket P1B with the configuration of the phyCORE-AT91M55800A as described above the following jumper settings are not functional or require special cabling:

Jumper	Setting	Description
JP1	*closed*[3]	Pin 2 of DB-9 socket P1B connected to TxD1 signal from phyCORE-AT91M55800A
JP2	closed	Pin 9 of DB-9 socket P1B connected with port PA28 (/PCS2) from phyCORE-AT91M55800A
JP3	open	Pin 7 of DB-9 socket P1B connected with port TxD2_RS232 from phyCORE-AT91M55800A
JP4	closed	Pin 4 of DB-9 socket P1B connected with port PA26 (/PCS0) from phyCORE-AT91M55800A
JP5	closed	Pin 6 of DB-9 socket P1B connected with port PA25 (MOSI) from phyCORE-AT91M55800A
JP6	open	Pin 8 of DB-9 socket P1B connected with port RxD2_RS232 from phyCORE-AT91M55800A
JP7	closed	Pin 1 of DB-9 socket P1B connected with port PA29 (/PCS3) from phyCORE-AT91M55800A
JP8	*closed*[3]	Pin 3 of DB-9 socket P1B connected to RxD1 signal from phyCORE-AT91M55800A

Table 39: Improper Jumper Settings for DB-9 Socket P1B (Third RS-232)

The voltage level on the RS-232 lines could destroy the phyCORE-AT91M55800A.

1 : Optional, only if all 3 serial interfaces are required on the DB-9 sockets P1.

2 : **Note:** This pin layout does **not** correspond to the standard pin assignment for RxD and TxD signals and requires use of a special RS-232 cable set.

3 : This jumper setting can be used and results in a socket P1B configuration where **both** signals for the second **and** the third RS-232 interface of the phyCORE-AT91M55800A are available.

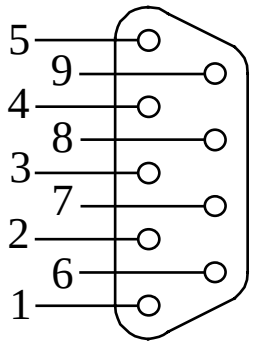
14.3.6 First CAN Interface at Plug P2A

Plug P2A is the lower plug of the double DB-9 connector at P2. P2A is connected to the first CAN interface (CAN0) of the phyCORE-AT91M55800A via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver populating the phyCORE-AT91M55800A is populated and the CAN signals from the module extend directly to plug P2A.

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of the DB-9 plug P2A is connected to CAN-L0 from on-board transceiver on the phyCORE module
JP32	2 + 3	Pin 7 of the DB-9 plug P2A is connected to CAN-H0 from on-board transceiver on the phyCORE module
JP11	open	Input at opto-coupler U4 on the phyCORE Development Board HD200 open
JP12	open	Output at opto-coupler U5 on the phyCORE Development Board HD200 open
JP13	open	No supply voltage to CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP18	open	No GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 40: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the phyCORE-AT91M55800A



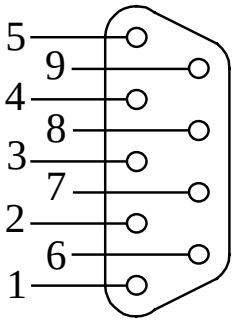
Pin 3:	GND	(Development Board Ground)
Pin 7:	CAN-H0	(not galvanically separated)
Pin 2:	CAN-L0	(not galvanically separated)
Pin 6:	GND	(Development Board Ground)

Figure 22: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on phyCORE-AT91M55800A, Front View)

2. No CAN transceiver is populating the phyCORE-AT91M55800A and Jumpers J14 and J15 are closed; CAN signals generated by the CAN transceiver (U2) on the Development Board extending to connector P2A **without galvanic seperation:**

Jumper	Setting	Description
JP31	1 + 2[1]	Pin 2 of the DB-9 plug P2A is connected to CAN-L0 from transceiver on the Development Board HD200
JP32	1 + 2[1]	Pin 7 of the DB-9 plug P2A is connected to CAN-H0 from transceiver on the Development Board HD200
JP11	2 + 4	Input at opto-coupler U4 on the phyCORE Development Board HD200 connected with CAN-H0/TxDCA of the phyCORE-AT91M55800A
JP12	2 + 4	Output at opto-coupler U5 on the phyCORE Development Board HD200 connected with CAN-L0/RxDCA of the phyCORE-AT91M55800A
JP13	2 + 3	Supply voltage to CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP18	1 + 2	GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 41: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board HD200



Pin 3: GND (Development Board Ground)
Pin 7: CAN-H0 (not galvanically separated)
Pin 2: CAN-L0 (not galvanically separated)
Pin 6: GND (Development Board Ground

Figure 23: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board)

[1]: Please make sure the CAN transceiver on the phyCORE-AT91M55800A is not populated and Jumpers J14 and J15 are closed (*refer to section 3.7 for details*).

Caution:

When using the DB-9 connector P2A as CAN interface and the CAN transceiver on the Development Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of DB-9 plug P2A connected with RxDCA of the phyCORE-AT91M55800A
JP32	2 + 3	Pin 7 of DB-9 plug P2A connected with TxDCA of the phyCORE-AT91M55800A
JP11	1 + 2	Input at opto-coupler U4 on the Development Board is connected to SPCK of the phyCORE-AT91M55800A
	2 + 3	Input at opto-coupler U4 on the Development Board is connected to A22 of the phyCORE-AT91M55800A
	open	Input at opto-coupler U4 on the Development Board not connected
JP12	1 + 2	Output at opto-coupler U5 on the Development Board is connected to MISO of the phyCORE-AT91M55800A
	2 + 3	Output at opto-coupler U5 on the Development Board is connected to A21 of the phyCORE-AT91M55800A
	open	Output at opto-coupler U5 on the Development Board not connected
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 connector P2A
JP39	see *Table 44*	CAN bus supply voltage reduction for CAN circuitry

Table 42: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on the Development Board)

3. The CAN transceiver is not populated on the phyCORE-AT91M55800A and Jumpers J14 and J15 are closed; CAN signals generated by the CAN transceiver (U2) on the Development Board extend to connector P2A **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP31	1 + 2	Pin 2 of DB-9 plug P2A connected with CAN-L0 from CAN transceiver U2 on the Development Board
JP32	1 + 2	Pin 7 of DB-9 plug P2A connected with CAN-H0 from CAN transceiver U2 on the Development Board
JP11	2 + 4[1]	Input at opto-coupler U4 on the Development Board connected to CAN-H0/TxDCA of the phyCORE-AT91M55800A
JP12	2 + 4[1]	Output at opto-coupler U5 on the Development Board connected to CAN-L0/RxDCA of the phyCORE-AT91M55800A
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP18	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A
JP39	see *Table 44*	CAN bus supply voltage reduction for CAN circuitry

Table 43: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board with Galvanic Separation

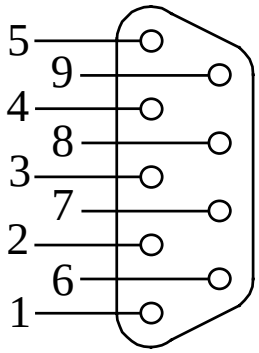
1: Please make sure the CAN transceiver on the phyCORE-AT91M55800A is not populated and Jumpers J14 and J15 are closed (*refer to section 3.7 for details*).

CAN Bus Voltage Supply Reduction via JP39:

Depending on the voltage level that is supplied over the CAN bus at P2A or P2B (VCAN_IN1+) JP39 must be configured in order to routed the applicable voltage to the CAN voltage regulator at U8 on the Development Board:

VCAN_IN+	**JP39**
7 V..18 V	1 + 2
18 V..23 V	2 + 3
23 V..28 V	open

Table 44: JP39 CAN Bus Voltage Supply Reduction



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN-H0 (galvanically separated)
Pin 2: CAN-L0 (galvanically separated)
Pin 6: VCAN-

Figure 24: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

Caution:

When using the DB-9 plug P2A as CAN interface, and the CAN transceiver on the Development Board with galvanic separation, the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP31	2 + 3	Pin 2 of DB-9 plug P2A connected with RxDCA of the phyCORE-AT91M55800A
JP32	2 + 3	Pin 7 of DB-9 plug P2A connected with TxDCA of the phyCORE-AT91M55800A
JP11	1 + 2	Input at opto-coupler U4 on the Development Board is connected to SPCK of the phyCORE-AT91M55800A
	2 + 3	Input at opto-coupler U4 on the Development Board is connected to A22 of the phyCORE-AT91M55800A
	open	Input at opto-coupler U4 on the Development Board not connected
JP12	1 + 2	Output at opto-coupler U5 on the Development Board is connected to MISO of the phyCORE-AT91M55800A
	2 + 3	Output at opto-coupler U5 on the Development Board is connected to A21 of the phyCORE-AT91M55800A
	open	Output at opto-coupler U5 on the Development Board not connected
JP13	2 + 3	Supply voltage for CAN transceiver and opto-coupler derived from local supply circuitry on the phyCORE Development Board HD200
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	see *Table 44*	Incorrect CAN bus supply voltage reduction for CAN circuitry

Table 45: Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on Development Board with Galvanic Separation)

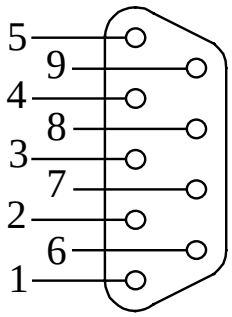
14.3.7 Second CAN Interface at Plug P2B

Plug P2B is the upper plug of the double DB-9 connector at P2. P2B is connected to the second CAN interface (CAN1) of the phyCORE-AT91M55800A via jumpers. Depending on the configuration of the CAN transceivers and their power supply, the following three configurations are possible:

1. CAN transceiver populating the phyCORE-AT91M55800A and the CAN signals from the module extend directly to plug P2B.

Jumper	Setting	Description
JP33	2 + 4	Pin 2 of the DB-9 plug P2B is connected to CAN-L1 from on-board transceiver on the phyCORE module
JP34	2 + 3	Pin 7 of the DB-9 plug P2B is connected to CAN-H1 from on-board transceiver on the phyCORE module
JP14	open	Input at opto-coupler U6 on the phyCORE Development Board HD200 open
JP15	open	Output at opto-coupler U7 on the phyCORE Development Board HD200 open
JP13	open	CAN transceiver and opto-coupler on the Development Board disconnected from supply voltage
JP18	open	No GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 46: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the phyCORE-AT91M55800A



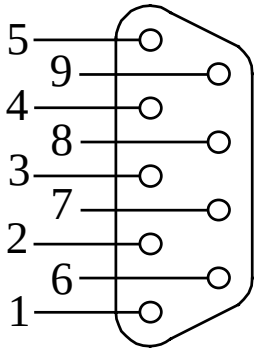
Pin 3:	GND	(Development Board Ground)
Pin 7:	CAN-H1	(not galvanically separated)
Pin 2:	CAN-L1	(not galvanically separated)
Pin 6:	GND	(Development Board Ground)

Figure 25: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on phyCORE-AT91M55800A, Front View)

2. No CAN transceiver is populating the phyCORE-AT91M55800A and Jumpers J16 and J17 are closed; CAN signals generated by the CAN transceiver (U3) on the Development Board extending to connector P2B **without galvanic seperation:**

Jumper	Setting	Description
JP33	2 + 3	Pin 2 of the DB-9 plug P2B is connected to CAN-L1 of CAN transceiver U3 of the Development Board HD200
JP34	1 + 2	Pin 7 of the DB-9 plug P2B is connected to CAN-H1 of CAN transceiver U3 of the Development Board HD200
JP14	2 + 4[1]	Input at opto-coupler U6 on the Development Board connected to CAN-H1/TxDCB of the phyCORE-AT91M55800A
JP15	2 + 4[1]	Output at opto-coupler U7 on the Development Board connected to CAN-L1/RxDCB of the phyCORE-AT91M55800
JP13	closed	CAN transceiver and opto-coupler on the Development Board connected with 5V supply voltage
JP18	closed	GND potential at CAN transceiver and opto-coupler on the phyCORE Development Board HD200
JP29	open	No power supply via CAN bus
JP39	open	No power supply via CAN bus

Table 47: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Development Board HD200



Pin 3: GND (Development Board Ground)
Pin 7: CAN-H0 (not galvanically separated)
Pin 2: CAN-L0 (not galvanically separated)
Pin 6: GND (Development Board Ground

Figure 26: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board)

1: Please make sure the CAN transceiver on the phyCORE-AT91M55800A is not populated and Jumpers J16 and J17 are closed (*refer to section 3.7 for details*).

Caution:
When using the DB-9 connector P2B as second CAN interface and the CAN transceiver on the Development Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP30	closed	Pin 8 at P2B is connected with TxD1_RS232 from the phyCORE-AT91M55800A
JP33	1 + 2	Pin 2 at P2B is connected with RxD1_RS232 from the phyCORE-AT91M55800A
	2 + 4	Pin 2 at P2B is connected with CAN_L1/RxDCB from the on-board CAN transceiver on the phyCORE-AT91M55800A
JP34	2 + 3	Pin 7 at P2B is connected with CAN_H1/TxDCB from the on-board CAN transceiver on the phyCORE-AT91M55800A
JP14	1 + 2	Input at opto-coupler U6 on the Development Board is connected to PB2 of the phyCORE-AT91M55800A
	2 + 3	Input at opto-coupler U6 on the Development Board is connected to A23 of the phyCORE-AT91M55800A
	open	Input at opto-coupler U6 on the Development Board not connected
JP15	1 + 2	Output at opto-coupler U7 on the Development Board is connected to PB0 of the phyCORE-AT91M55800A
	2 + 3	Output at opto-coupler U7 on the Development Board is connected to A20 of the phyCORE-AT91M55800A
	open	Output at opto-coupler U7 on the Development Board not connected
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 connector P2A
JP39	see *Table 44*	CAN bus supply voltage reduction for CAN circuitry

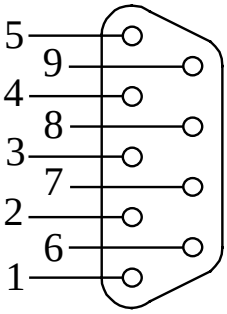
Table 48: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on the Development Board)

3. The CAN transceiver is not populating the phyCORE-AT91M55800A and Jumpers J16 and J17 are closed; CAN signals generated by the CAN transceiver (U3) on the Development Board extend to connector P2B **with galvanic separation.** This configuration requires connection of an external CAN supply voltage of 7 to 13 V. The external power supply must be **only** connected to either P2A **or** P2B.

Jumper	Setting	Description
JP33	2 + 3	Pin 2 of DB-9 plug P2B connected with CAN-L1 from CAN transceiver U3 on the Development Board
JP34	1 + 2	Pin 7 of DB-9 plug P2B connected with CAN-H1 from CAN transceiver U3 on the Development Board
JP14	2 + 4[1]	Input at opto-coupler U6 on the Development Board connected to CAN-H1/TxDCB of the phyCORE-AT91M55800A
JP15	2 + 4[1]	Output at opto-coupler U7 on the Development Board connected to CAN-L1/RxDCB of the phyCORE-AT91M55800A
JP13	1 + 2	Supply voltage for CAN transceiver and opto-coupler on the Development Board derived from external source (CAN bus) via on-board voltage regulator
JP18	open	CAN transceiver and opto-coupler on the Development Board disconnected from local GND potential
JP29	closed	Supply voltage for on-board voltage regulator from pin 9 of DB-9 plug P2A
JP39	see *Table 44*	CAN bus supply voltage reduction for CAN circuitry

Table 49: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Development Board with Galvanic Separation

1: Please make sure the CAN transceiver on the phyCORE-AT91M55800A is not populated and Jumpers J16 and J17 are closed (*refer to section 3.7 for details*).



Pin 9: VCAN+

Pin 3: VCAN-
Pin 7: CAN-H1 (galvanically separated)
Pin 2: CAN-L1 (galvanically separated)
Pin 6: VCAN-

Figure 27: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

Caution:

When using the DB-9 plug P2B as second CAN interface, and the CAN transceiver on the Development Board with galvanic separation, the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP30	closed	Pin 8 at P2B is connected with TxD1_RS232 from the phyCORE-AT91M55800A
JP33	1 + 2	Pin 2 at P2B is connected with RxD1_RS232 from the phyCORE-AT91M55800A
	2 + 4	Pin 2 at P2B is connected with CAN_L1/RxDCB from the phyCORE-AT91M55800A
JP34	2 + 3	Pin 7 at P2B is connected with CAN_H1/TxDCB from the phyCORE-AT91M55800A
JP14	1 + 2	Input at opto-coupler U6 on the Development Board is connected to PB2 of the phyCORE-AT91M55800A
	2 + 3	Input at opto-coupler U6 on the Development Board is connected to A23 of the phyCORE-AT91M55800A
	open	Input at opto-coupler U6 on the Development Board not connected
JP15	1 + 2	Output at opto-coupler U7 on the Development Board is connected to PB0 of the phyCORE-AT91M55800A
	2 + 3	Output at opto-coupler U7 on the Development Board is connected to A20 of the phyCORE-AT91M55800A
	open	Output at opto-coupler U7 on the Development Board not connected
JP13	2 + 3	Supply voltage for CAN transceiver and opto-coupler derived from local supply circuitry on the phyCORE Development Board HD200
JP18	closed	CAN transceiver and opto-coupler on the Development Board connected with local GND potential
JP29	open	No power supply via CAN bus
JP39	*see Table 44*	Incorrect CAN bus supply voltage reduction for CAN circuitry

Table 50: Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on Development Board with Galvanic Separation)

14.3.8 Programmable LED D3

The phyCORE Development Board HD200 offers a programmable LED at D3 for user implementations. This LED can be connected to port pin P2.0 of the phyCORE-AT91M55800A which is available via signal GPIO0 (JP17 = closed). A low-level at port pin PA0 causes the LED to illuminate, LED D3 remains off when writing a high-level to PA0.

Jumper	Setting	Description
JP17	closed	Port pin PA0 (GPIO0) of the AT91M55800A controls LED D3 on the Development Board

Table 51: JP17 Configuration of the Programmable LED D3

14.3.9 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

As described in *section 14.1*, all signals from the phyCORE-AT91M55800A extend in a strict 1:1 assignment to the Expansion Bus connector X2 on the Development Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Development Board at X2.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X2 on the Development Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

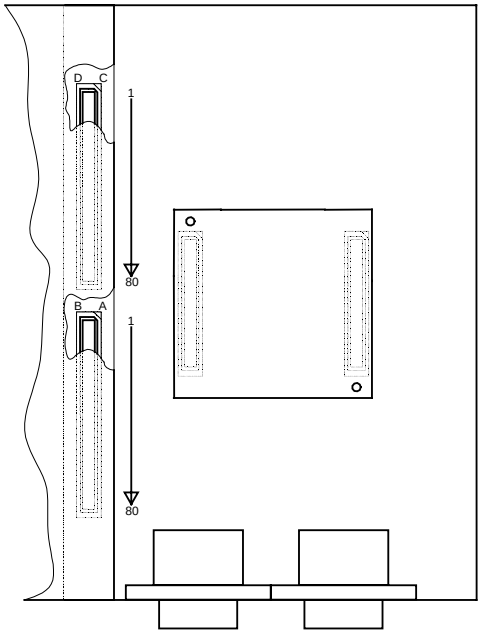


Figure 28: Pin Assignment Scheme of the Expansion Bus

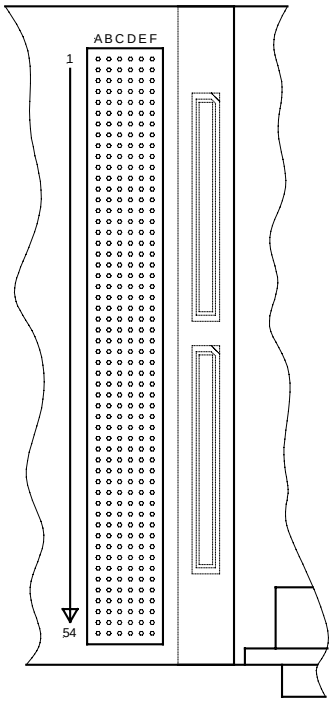


Figure 29: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-AT91M55800A, in conjunction with the Expansion Bus (X2) on the Development Board and the patch field on an expansion board, is as follows:

Signal	phyCORE Module	Expansion Bus	Patch Field
D0	18B	18B	33F
D1	19A	19A	34A
D2	20A	20A	34E
D3	20B	20B	34B
D4	21A	21A	34D
D5	21B	21B	34F
D6	22B	22B	35A
D7	23A	23A	35E
D8	28B	28B	37C
D9	29A	29A	37E
D10	30A	30A	37B
D11	30B	30B	37F
D12	31A	31A	38A
D13	31B	31B	38C
D14	32B	32B	38E
D15	33A	33A	38B
A0	8B	8B	30B
A1	9A	9A	30D
A2	10A	10A	30F
A3	10B	10B	31A
A4	11A	11A	31E
A5	11B	11B	31B
A6	12B	12B	31F
A7	13A	13A	32A
A8	13B	13B	32C
A9	14A	14A	32E
A10	15A	15A	32B
A11	15B	15B	32F
A12	16A	16A	33A
A13	16B	16B	33C
A14	17B	17B	33E
A15	18A	18A	33B

Table 52: Pin Assignment Data/Address Bus for the phyCORE-AT91M55800A / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
A16	23B	23B	35B
A17	24A	24A	35D
A18	25A	25A	35F
A19	25B	25B	36A
A20	26A	26A	36E
A21	26B	26B	36B
A22	27B	27B	36F
A23	28A	28A	37A
/CS0	5A	5A	29E
/CS1	5B	5B	29B
/CS2	6A	6A	29D
/CS3	6B	6B	29F
/CS4	35A	35A	39E
/CS5	35B	35B	39B
/CS6	36A	36A	39D
/CS7	36B	36B	39F
/RD	7B	7B	30A
/WR	8A	8A	30E
/WAIT	34A	34A	39A
/RESIN	10D	10D	3F
/RESET	10C	10C	3D
/SHDN	11C	11C	4E
WAKEUP	20C	20C	7A
/WDOVF	8C	8C	3E
AD0	50C	50C	17A
AD1	49C	49C	16F
AD2	48D	48D	16B
AD3	48C	48C	16E
AD4	47D	47D	16C
AD5	46D	46D	16A
AD6	46C	46C	15F
AD7	45D	45D	15B
DA0	43C	43C	14F
DA1	43D	43D	15A

Table 53: Pin Assignment Address/Control Bus and Analog Port for the phyCORE-AT91M55800A / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
PA0 / TCLK3	11D	11D	4A
PA1 / TIOA3	12D	12D	4B
PA2 / TIOB3	13C	13C	4F
PA3 / TCLK4	13D	13D	5A
PA4 / TIOA4	14C	14C	5C
PA5 / TIOB4	15C	15C	5E
PA6 / TCLK5	15D	15D	5B
PA7 / TIOA5	16C	16C	5F
PA8 / TIOB5	41C	41C	14A
PA9 / IRQ0	2B	2B	28E
PA10 / IRQ1	3A	3A	28B
PA11 / IRQ2	3B	3B	28F
PA12 / IRQ3	4A	4A	29A
PA13 / FIQ	41D	41D	14E
PA14 / SCK0	19C	19C	6F
PA15 / TxD0	17D	17D	6C
PA16 / RxD0	16D	16D	6A
PA17 / SCK1	9C	9C	3B
PA18 / TxD1 / /TRI	23C[1]	23C[1]	8A
PA19 / RxD1	21C[2]	21C[1]	7B
PA20 / SCK2	25D	25D	8F
PA21 / TxD2	25C[3]	25C[3]	8D
PA22 / RxD2	24C[4]	24C[4]	8B
PA23 / SPCK	28D	28D	10A
PA24 / MISO	27D	27D	9B
PA25 / MOSI	28C	28C	9F
PA26 / /PCS0 / /SS	26C	26C	9A
PA27 / /PCS1	26D	26D	9E
PA28 / /PCS2	29C	29C	10C
PA29 / /PCS3	30C	30C	10E

Table 54: Pin Assignment Port PA for the phyCORE-AT91M55800A / Development Board / Expansion Board

[1] : Check configuration of Jumper J39 on the phyCORE-AT91M55800A, *refer to section 3.19*.
[2] : Check configuration of Jumper J38 on the phyCORE-AT91M55800A, *refer to section 3.19*.
[3] : Check configuration of Jumper J10 on the phyCORE-AT91M55800A, *refer to section 3.3*.
[4] : Check configuration of Jumper J11 on the phyCORE-AT91M55800A, *refer to section 3.3*.

Signal	phyCORE Module	Expansion Bus	Patch Field
PB0	30D	30D	10B
PB1	31C	31C	10F
PB2	31D	31D	11A
PB3 / IRQ4	32D	32D	11C
PB4 / IRQ5	33D	33D	11B
PB5 / IRQ6	50B	50B	44B
PB6 / AD0TRIG	45C	45C	15E
PB7 / AD1TRIG	44C	44C	15C
PB8	37B	37B	40A
PB9	38A	38A	40E
PB10	38B	38B	40B
PB11	39A	39A	40D
PB12	40A	40A	40F
PB13	40B	40B	41A
PB14	41A	41A	41E
PB15	41B	41B	41B
PB16	42B	42B	41F
PB17	43A	43A	42A
PB18 / BMS	43B	43B	42C
PB19 / TCLK0	44A	44A	42E
PB20 / TIOA0	45A	45A	42B
PB21 /TIOB0	45B	45B	42F
PB22 / TCLK1	46A	46A	43A
PB23 / TIOA1	46B	46B	43C
PB24 / TIOB1	47B	47B	43E
PB25 / TCLK2	48A	48A	43B
PB26 / TIOA2	48B	48B	43F
PB27 / TIOB2	49A	49A	44A

Table 55: Pin Assignment Port PB for the phyCORE-AT91M55800A / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
CAN-H0	21D	21D	7D
CAN-L0	20D	20D	7E
CAN-H1	18C	18C	6E
CAN-L1	18D	18D	6B
RxD0_RS232	22D	22D	7F
TxD0_RS232	23D	23D	8E
RxD1_RS232	21C	21C	7B
TxD1_RS232	23C	23C	8A
RxD2_RS232	24C	24C	8B
TxD2_RS232	25C	25C	8D
LAN_LED	33C	33C	11E
LINK_LED	34C	34C	11F
RxD-	35C	35C	12A
RxD+	35D	35D	12E
TxD-	36C	36C	12B
TxD+	36D	36D	12D
JTAGSEL	37D	37D	12F
/TRST	39C	39C	13B
TMS	40D	40D	13F
TDO	38D	38D	12E
TDI	38C	38C	13A
TCK	40C	40C	13D

Table 56: Pin Assignment Interface Signals for the phyCORE-AT91M55800A / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
VCC	1C, 2C, 1D, 2D	1C, 2C, 1D, 2D	1A, 1C
VCC2	4C, 5C	4C, 5C	2A, 1B
XIN	1A	1A	28A
MCKO	1B	1B	28C
VPD	6D	6D	2D
VBAT	6C	6C	2B
ADVREF	50D	50D	17E
DAVREF	42D	42D	14B
VAGND	42C, 47C, 44D, 49D	42C, 47C, 44D, 49D	connected to GND
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A,42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 42D, 47D, 52D, 57D, 62D, 67D, 72D, 77D	3C, 4C, 7C, 8C, 9C, 12C, 13C, 14C, 17C, 18C, 19C, 22C, 23C, 24C, 27C, 29C, 30C, 31C, 34C, 35C, 36C, 39C, 40C, 41C, 44C, 45C, 46C, 49C, 50C, 51C, 54C, 4D, 5D, 6D, 9D, 10D, 11D, 14D, 15D, 16D, 9D, 20D, 21D, 24D, 25D, 26D, 28D, 31D, 32D, 33D, 36D, 37D, 38D, 41D, 42D, 43D, 46D, 47D, 48D, 51D, 52D, 53D, 1E, 2E, 1F

Table 57: Pin Assignment Power Supply for the phyCORE-AT91M55800A / Development Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
NC	50A, 4D, 5D, 7D, 8D	50A, 51A, 53A, 54A, 55A, 56A, 58A, 59A, 60A, 61A, 63A, 64A, 65A, 66A, 68A, 69A, 70A, 71A, 73A, 74A, 75A, 76A, 78A, 79A, 80A 51B, 53B, 54B, 55B, 56B, 58B, 59B, 60B, 61B, 63B, 64B, 65B, 66B, 68B, 69B, 70B, 71B, 73B, 74B, 75B, 76B, 78B, 79B, 80B 51C, 53C, 54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C, 73C, 74C, 75C, 76C, 78C, 79C, 80C 4D, 5D, 7D, 8D, 51D, 53D, 54D, 55D, 56D, 58D, 59D, 60D, 61D, 63D, 64D, 65D, 66D, 68D, 69D, 70D, 71D, 73D, 74D, 75D, 76D, 78D, 79D, 80D	18A, 19A, 20A, 21A, 22A, 23A 24A, 25A, 26A, 27A, 45A, 46A, 47A, 48A, 49A, 50A, 51A, 52A, 53A, 54A 17B, 18B, 19B, 20B, 21B, 22B, 23B, 24B, 25B, 26B, 27B, 45B, 46B, 47B, 48B, 49B, 50B, 51B, 52B, 53B, 54B 20C, 21C, 25C, 26C, 47C, 48C, 52C, 53C 17D, 18D, 22D, 23D, 27D, 44D 45D, 49D, 50D, 54D 18E, 19E, 20E, 21E, 22E, 23E, 24E, 25E, 26E, 27E, 45E, 46E, 47E, 48E, 49E, 50E, 51E, 52E, 53E, 54E 17F, 18F, 19F, 20F, 21F, 22F, 23F, 24F, 25F, 26F, 27F, 44F, 45F, 46F, 47F, 48F, 49F, 50F, 51F, 52F, 53F, 54F

Table 58: Unused Pins on the phyCORE-AT91M55800A / Development Board / Expansion Board

14.3.10 Battery Connector BAT1

The mounting space BAT1 (see PCB stencil) is provided for connection of a battery that buffers the RTC on the phyCORE-AT91M55800A. In the event of a VCC operating voltage failure the RTC is automatically supplied with power from the connected battery. There is also the option of buffering the SRAMs with an external battery. This optional setting is configured with Jumper J25 (*see section 3.12*). In most cases an SRAM buffer is not recommended since the SRAM devices draw their operating current from VBAT during runtime of the module and therefore cause rapid battery discharge. The optional battery required for the RTC buffering (*refer to section 10*) is available through PHYTEC (order code BL-003).

14.3.11 DS2401 Silicon Serial Number

Communication to a DS2401 Silicon Serial Number can be implemented in various software applications for the definition of a node address or as copy protection in networked applications. The DS2401 can be soldered on space U10 or U9 on the Development Board, depending on the type of device packaging being used.

The Silicon Serial Number Chip mounted on the phyCORE Development Board HD200 can be connected to port pin PA1 of the AT91M55800A available at GPIO1 (JP19 = closed).

Jumper	Setting	Description
JP19	closed	Port pin P2.1 (GPIO1) of the AT91M55800A is used to access the Silicon Serial Number

Table 59: JP19 Jumper Configuration for Silicon Serial Number Chip

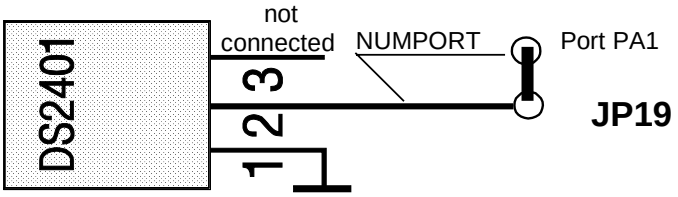


Figure 30: Connecting the DS2401 Silicon Serial Number

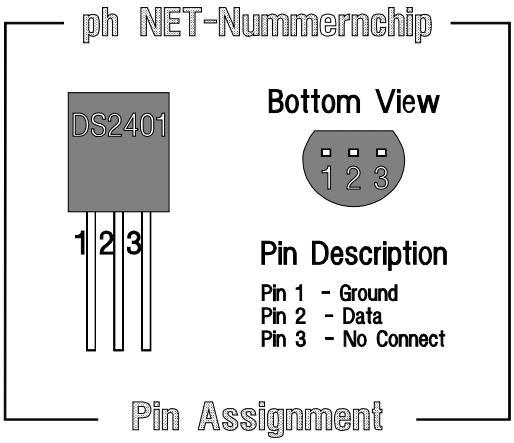


Figure 31: Pin Assignment of the DS2401 Silicon Serial Number

14.3.12 Pin Header Connector X4

The pin header X4 on the Development Board enables connection of an optional modem power supply. Connector X4 supplies 5 V = at pin 1 and provides the phyCORE Development Board HD200 GND potential at pin 2. The maximum current draw depends on the power adapter used. We recommend the use of modems with less than 250 mA current draw.

15 Ethernet Port

The phyCORE Development Board HD200 provides a 10-pin header connector at X7 for mounting the PHYTEC Ethernet transformer module. The optional add-on module is available through PHYTEC (order code EAD-001 or EAD-001-3V). This allows for direct connection of the phyCORE-AT91M55800A with populated Ethernet controller mounted on a Development Board HD200 to a 10Base-T network.

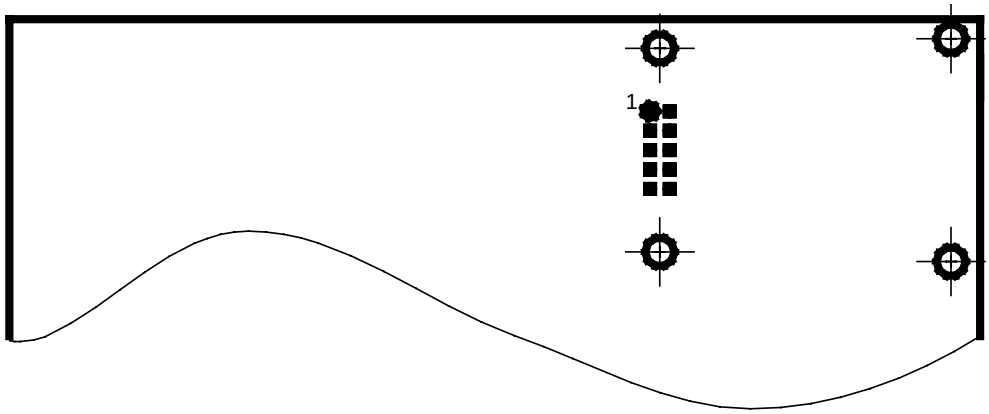


Figure 32: Ethernet Transformer Module Connector

The pinout for the Ethernet transformer connector is shown below:

Pin#	Function	Note
1	ETH_LanLED	Make sure JP37 on the Development Board is closed at position 1+2.
2	ETH_LinkLED	Make sure JP38 on the Development Board is closed at position 1+2.
3	VCC	
4	ETH_TxD+	
5	ETH_TxD-	
6	GND	
7	ETH_RxD+	
8	ETH_RxD-	
9	GND	
10	VCC	

Table 60: Ethernet Transformer Connector Pinout

16 Revision History

Date	Version numbers	Changes in this manual
06-Jun-2002	Manual L-618e_0 PCM-014 PCB# 1192.0 PCM-997-V2 PCB# 1179.3	First draft, Preliminary documentation.
17-Jul-2002	Manual L-618e_1 PCM-014 PCB# 1192.1 PCM-997-V2 PCB# 1179.3	Major changes due to hardware redesign. Various subsections in section 3, Jumpers, added. Improved description in Section 5 for memory models. Debug Interface section added.
21-Nov-2002	Manual L-618e_2 PCM-014 PCB# 1192.2 PCM-997-V2 PCB# 1179.3	New images in Figure 5 to reflect new PCB version. Description for J27 and J40 in section 3 added, J10 and J39 revised. Description in Section 5 for memory configuration added. Description in Section 10 for JTAG interfaces added. New images in Figure 8, Physical Dimensions. Minor changes in Section 14 for default configuration.
11-Feb-2003	Manual L-618e_3 PCM-014 PCB# 1192.2 PCM-997-V2 PCB# 1179.4	Section 3.18 /WAIT signal revised. New section 9 added describing the Ethernet controller. Section 14 adapted to describe Development Board HD200 (PCM-997-V2) with PCB# 1179.4. Sections 14.3.6 and 14.3.7 expanded to describe galvanic seperation of CAN bus signals. Section 15, Ethernet Port, added. This revision history table added.

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