miniMODUL-537/509

Hardware Manual

Edition February 2003

A product of a PHYTEC Technology Holding company

In this manual are descriptions for copyrighted products that are not explicitly indicated as such. The absence of the trademark (™) and copyright (©) symbols does not imply that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual.

The information in this document has been carefully checked and is believed to be entirely reliable. However, PHYTEC Meßtechnik GmbH assumes no responsibility for any inaccuracies. PHYTEC Meßtechnik GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product. PHYTEC Meßtechnik GmbH reserves the right to alter the information contained herein without prior notification and accepts no responsibility for any damages which might result.

Additionally, PHYTEC Meßtechnik GmbH offers no guarantee nor accepts any liability for damages arising from the improper usage or improper installation of the hardware or software. PHYTEC Meßtechnik GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 info@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

3rd Edition: February 2003

Index of Figures

Index of Tables

Preface

This miniMODUL-537/509 Hardware Manual describes the board's design and functions. Precise specifications for the SAB80C537 or C509 microcontroller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC miniMODUL-537/509

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The miniMODUL-537/509 is one of a series of PHYTEC nano/micro/miniMODULs which can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit controllers in two ways:

(1) as the basis for Starter Kits in which user-designed hardware can be implemented on a wrap-field around the controller and

(2) as insert-ready, fully functional micro- and miniMODULes which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The miniMODUL-537/509 is a continuation of PHYTEC's successful line of credit card-sized microcomputers. The core of the miniMODUL-537 version is the Infineon SAB80C537 8-bit controller, which is closely compatible to the 80C535 yet boasts the following integrated hardware additions: 4 timers, a 12-channel A/D-converter, two serial interfaces, a Watchdog-Timer, eight data-pointers, six ports and a high-performance arithmetic unit. The miniMODUL-509 version is based on the 80C509 controller which, in turn, extends the functionality of the C537. The C509 has a standard internal frequency booster which doubles its clock speed from 12 to 24 MHz. Its maximum clock frequency of 16 MHz allows it to attain the processing speed of an 8032 board running at a 32 MHz frequency (delivering an instruction cycle in 375 ns). It also offers 3 kByte on-chip RAM and Boot-ROM, as well as a 15-bit A/D-converter with 10-bit resolution. *Refer to the corresponding Controller User's Manual for detailed information.*

The module itself features 32 kByte SRAM and 128 kByte Flash, which can be programmed on-board using the PHYTEC FlashTools. All board components are addressable, with signals available at the pin rows aligning three edges of the board. The miniMODUL-509/537 can also accommodate an external address decoder. One of two RS-232 serial interfaces can be optionally configured as an RS-485 transceiver, hence allowing the module to be networked with other boards with RS-485 connectivity.

The module is easily programmable with the included 8051-compatible evaluation software development tools. These versatile on-chip and peripheral characteristics of the miniMODUL-537/509 render the module a complete microprocessor-system. Insertion of the miniMODUL-537/509 into a project allows engineers to forgo development of a digital microprocessor system to be embedded within application hardware, hence shortening development time horizons.

The miniMODUL-537/509 can also be inserted as a "big chip" into application hardware. Compare the cost-performance of PHYTEC's insert-ready miniMODUL-537/509 with the development, design and testing costs of your internal development.

This Hardware Manual describes the features and functions of the miniMODUL-537/509 with the PCB revision #1108.2.

The miniMODUL-537/509 offers the following features:

- SBC in credit card-size dimensions (55 x 85 mm) achieved through advanced SMD technology
- populated with Infineon 8051-compatible SAB80C509 in a QFP-100 socket or C537 controller in a PLCC-84 socket
- improved interference safety through multi-layer technology
- controller signals and ports extend to standard-width (2.54 mm) pins aligning board edges, allowing the board to be plugged into any target application like a "big chip"
- requires a single low power supply 5 VDC / typ. < 110 mA
- 128 (to 512) kByte Flash on-board (PLCC)
- on-board Flash programming, no dedicated Flash programming voltage required through use of 5 V Flash devices
- 32 (to 160) kByte RAM on-board (SMD)
- 32 kByte E²PROM (SMD) can also be mounted on the board
- supplemental 3 kByte XRAM on-chip and BOOT-ROM with the C509
- flexible software-configured address decoding through complex logic device
- bank latches for Flash and RAM integrated in address decoder
- serial interfaces via RS-232 (one of which is optionally configurable as an RS-485 interface to enable networking)
- choice of three available Real-Time Clock devices: RTC-8583, RTC-8564 or RTC-72423
- up to 32 kByte E²PROM or 8 kByte FRAM
- SRAM and Real-Time Clock buffered by external battery
- free Chip Select signals for easy connection external peripherals
- operates within a standard range of 0 to 70 degrees C°.

1.1 Block Diagram

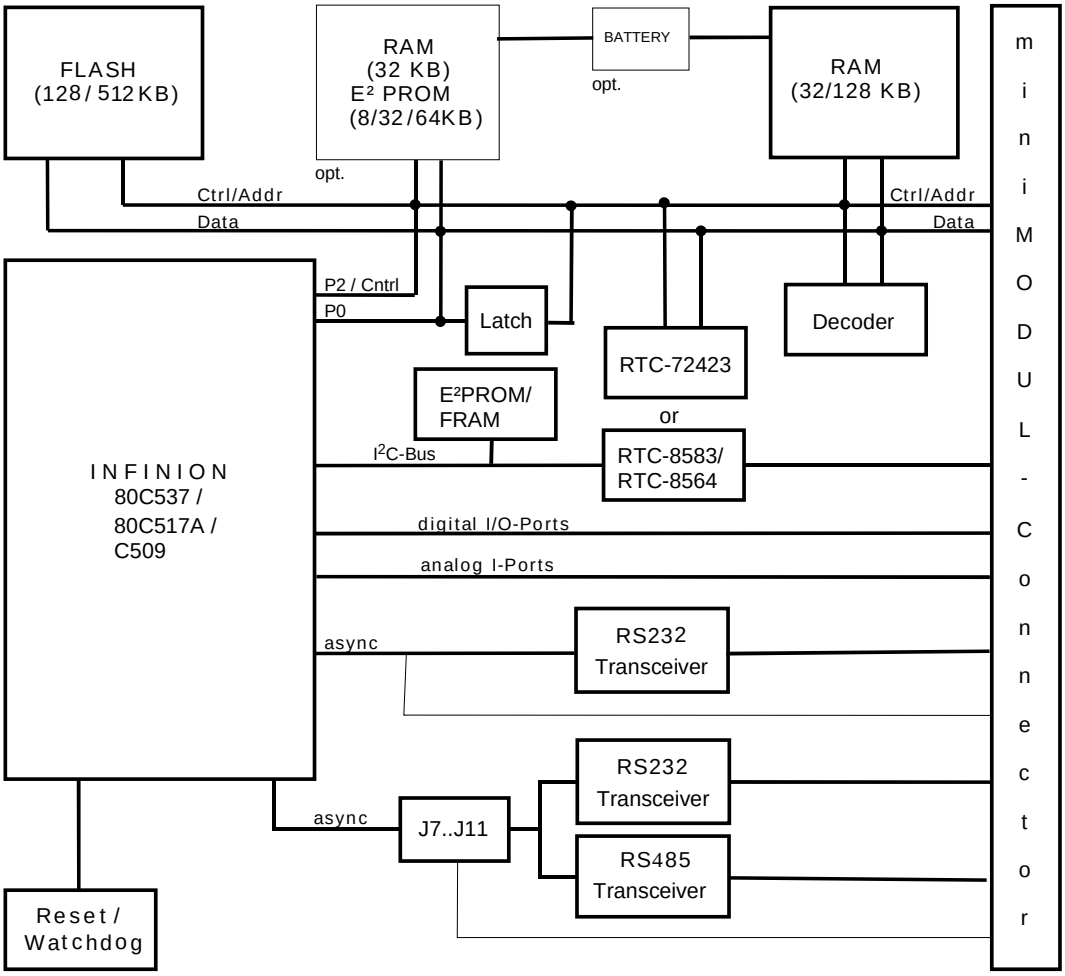


Figure 1: Block Diagram

1.2 Overview of the miniMODUL-537/509

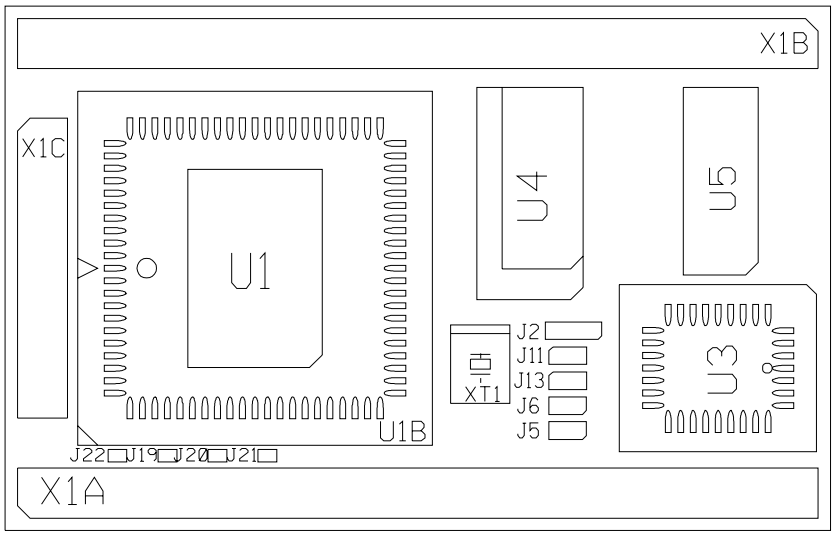


Figure 2: View of the miniMODUL-537/509 (Controller Side)

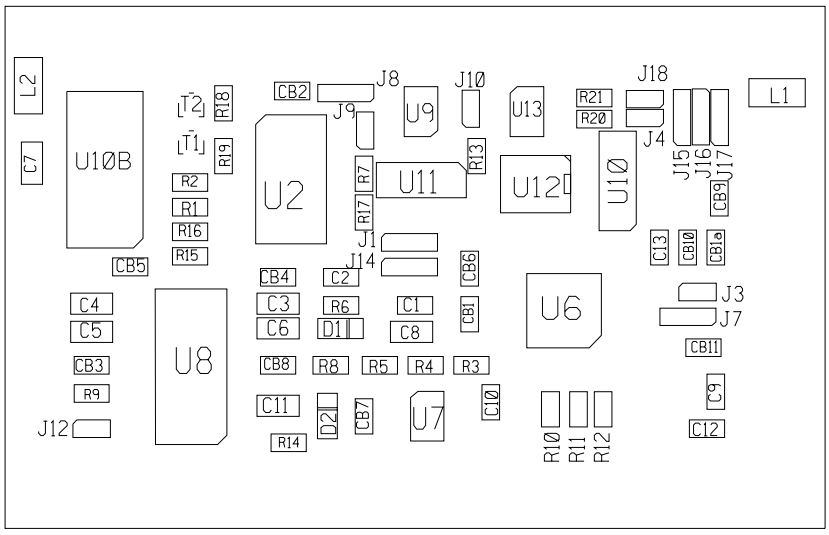


Figure 3: View of the miniMODUL-537/509 (Bottom Side)

2 Pinout

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to standard-width (2.54 mm) pin rows lining three sides the board (referred to as miniMODUL-Connector). This allows the board to be plugged into any target application like a "big chip". *Table 1* provides an overview of the pinout of the miniMODUL-connector

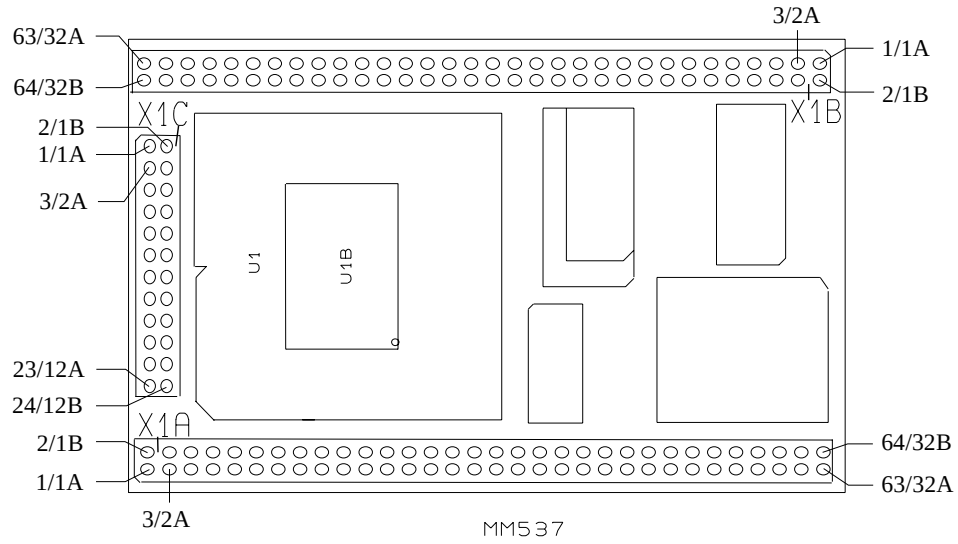


Figure 4: Pinout of the miniMODUL-537/509

Pin #	Connection	Comments
Pin row X1A		
1, 2/ 1A, 1B	NC	Not used
3..10/ 2A..5B	P4.0...P4.7	Port 4
11/ 6A	MDIS	Memory Disable input for U4 and U5
12/ 6B	/PSEP	separable Program-Store-Enable-signal of the controller
13/ 7A	/WRP	separable /WR-signal of the controller[1]
14/ 7B	/RDP	separable /RD-signal of the controller[1]
15..20/ 8A..10B	P3.0...P3.5	Port 3
21/ 11A	/WR , P3.6	separable /WR-signal of the module[1]
22/ 11B	/RD , P3.7	separable /RD-signal of the module[1]
23..30/ 12A 15B	P1.7...P1.0	Port 1
31/ 16A	/PSEN	separable Program Store Enable signal of the module[1]
32/ 16B	VPD	Voltage output for external buffer
33/ 17A	RES	Reset output of the module
34/ 17B	/RES	separable Reset input/output of the module[1]
35/ 18A	/CS1	pre-decoded Chip Select signal #1
36/ 18B	/CS2	pre-decoded Chip Select signal #2
37/ 19A	/CS3	pre-decoded Chip Select signal #3
38/ 19B	/PFO	Power-Fail Output
39/ 20A	PFI	Power-Fail Input
40/ 20B	/HPD	optional HWPD-Input for the C509/C517A
41, 43, 51, 52/ 21A, 22A, 26A, 26B	TI1...TI4	Transmitter inputs 1-4 of the RS-232 transceiver (TI1 and TI2 connected via Jumpers J5 and J8 to the serial interface of the controller)
42/ 21B	VBAT	Input for connection to external buffer battery
44, 54, 50/ 22B, 27B, 25B	RO1...RO3	Receiver outputs 1-3 of the RS-232 transceiver (RO1 and RO2 are connected via Jumpers J6 and J7 to the serial interface of the controller)
45 ,55 ,49/ 23A, 28A, 25A	RI1...RI3	Receiver inputs 1-3 of the RS-232 transceiver
47, 46, 48, 56/ 24A, 23B, 24B, 28B	TO1...TO4	Transmitter outputs 1-4 of the RS-232 transceiver
53/ 27A	RSDIS	RS-232 transceiver Disable input
57/ 29A	ALE	Address Latch Enable output
58/ 29B	/RESP	separable Reset signal of the controller[1]
59/ 30A	/CSRTC	Chip Select signal of RTC-72423 (connected via Jumper J13 to /CS1
60/ 30B	/IRTC	Interrupt output of both RTC chips
61/ 31A	/RESI	/Reset input of the module
62/ 31B	WDP	Watchdog input of the module
63, 64/ 32A, 32B	NC	not used

[1]: In order to implement an emulator, the controller signals /*XX*P can be separated from the /XX signals used in the module, enabling external input. Applicable signals are /PSEN, /RD, /WR and /RES.

Pin #	Connection	Comments
Pin row X1B		
1, 2/ 1A, 1B	VCC	Voltage input +5 V
3..10/ 2A..5B	AD7...AD0	Data bus (Port 0), multiplexed with low byte of address bus
11..18/ 6A..9B	A7...A0	Address bus (low byte)
19, 20....26/ / 10A, 10B..13B	A9 ,A8, A11, A10, A13, A12, A15, A14	Address bus (high byte)
27/ 14A	PRGEN	Program Enable input (only C509)
28/ 14B	NC	Not used
29/ 15A	DE	Data Enable input of the RS-485 transceiver (connected via pin 13 to U11)
30/ 15B	D	Data input of the RS-485 transmitter (connected via Jumper J8 to the serial interface of the controller)
31/ 16A	B	differential B-line of the RS-485 transceiver
32/ 16B	R	Data output of the RS-485 transceiver (connected via Jumper J7 to the serial interface of the controller)
33/ 17A	A	differential A-line of the RS-485 transceiver
34/ 17B	/R	inverted Data output of the RS-485 receiver (connected via Jumper J11 to P3.2 of the controller)
35/ 18A	/DE	inverted Data Enable input of the RS-485 transmitter (connected via Jumper J9 with P5.1 of the controller)
36/ 18B	/RE	Receive Enable input of the RS-485 receiver (connected via Jumper J10 to GND)
37..44/ 19A 22B	P9.7...P9.0	Port 9 (of the C509 controller)
45..52/ 23A 26B	P5.7...P5.0	Port 5
53/ 27A	/RO	Reset Output of the controller
54/ 27B	/PE	Watchdog Timer/Power-Save mode of the controller (connected via Jumper J3 to GND)
55..62/ 28A 31B	P6.0...P6.7	Port 6
63, 64/ 32A, 32B	GND	Ground 0 V.
Pin row X1C		
1, 5, 9, 13, 15, 17, 19, 21/ 1A, 3A, 5A, 7A, 8A, 9A, 10A, 11A	AGND	Analog Ground 0 V
3, 7, 11/ 2A, 4A, 6A	P8.4 ..P8.6/ AN12...AN14	Analog inputs AN12...AN14 (only for the C509 controller)
8, 6, 4, 2, 24, 22, 20, 18, 16, 14, 12, 10/ 4B, 3B, 2B, 1B, 12B, 11B, 10B, 9B, 8B, 7B, 6B, 5B	P8.3..P8.0, P7.7.. P7.0/ AN11.AN0	Analog inputs AN11...AN0
23/ 12A	AREF	Analog Reference Voltage + 5 V

Table 1: Pin Description of the miniMODUL-537/509

3 Jumpers

For configuration purposes, the miniMODUL-537/509 has 22 soldering jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and *Figure 7* indicate the location of the jumpers on the board.

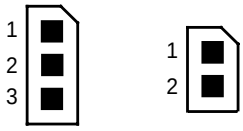


Figure 5: Numbering of the Jumper Pads

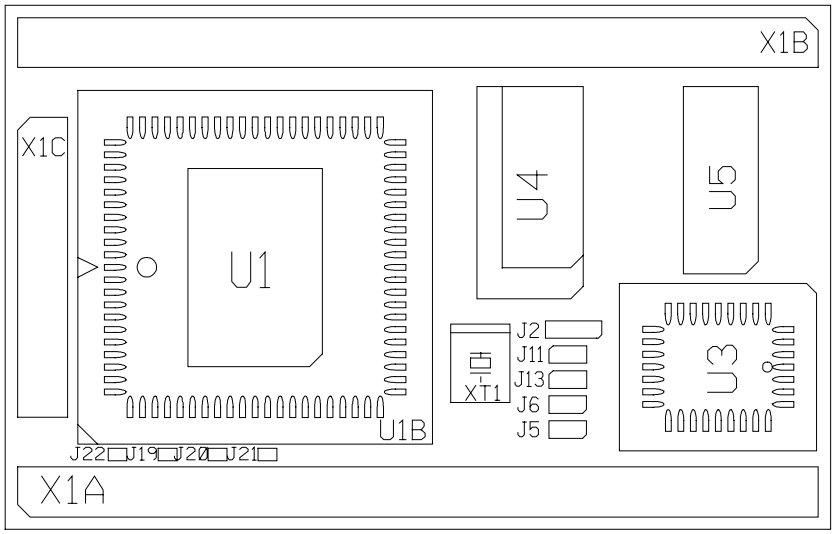


Figure 6: Location of the Jumpers (Controller Side)

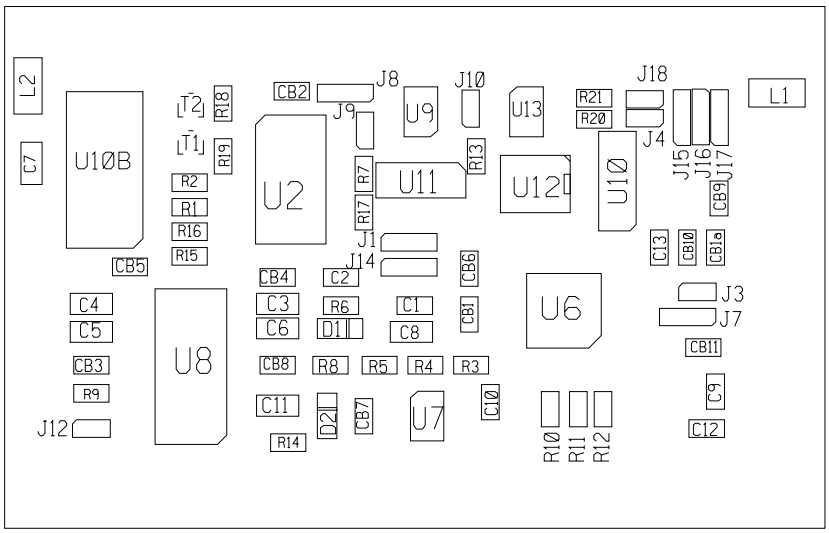


Figure 7: Location of the Jumpers (Bottom Side)

3.1 J1 Internal or External Program Memory

At the time of delivery, Jumper J1 is closed at position 1+2. This default configuration means that the program stored in the external program memory is executed after a hardware reset. In order to allow the execution of a specific controller's internal program memory, Jumper J1 must be closed at position 2+3.

The following configurations are possible:

Code Fetch Selection	J1
Execution from external program memory	1 + 2*
Execution from internal program memory	2 + 3

* = Default setting

Table 2: J1 Code Fetch Selection

3.2 J2 SRAM/E²PROM (U5) Supply Voltage

The devices at U5 can be connected to VCC or VPD using Jumper J2. If U5 is populated with a serial E²PROM the voltage supply pins must be connected to VCC (J2 = 1+2). This is necessary to avoid fast battery discharge. Alternatively, if an SRAM device populates U5, the circuit supply pins can be applied to the battery voltage VPD for purposes of data buffering in case VCC is turned off.

The following configurations are possible:

Supply Voltage for SRAM/E²PROM at U5	J2
E²PROM/FRAM at U5 supplied with VCC	1 + 2*
E²PROM/FRAM at U5 supplied with VPD	2 + 3

*= Default setting

Table 3: J2 SRAM/E²PROM Supply Voltage Configuration

3.3 J3 Power-Saving Modes / Watchdog Timer

Opening Jumper J3 deactivates the Power-Saving mode. This also automatically starts the Watchdog timer after a hardware reset. Upon delivery, the Watchdog timer is deactivated. Jumper J3 allows activation of either the timer or the Power-Saving mode.

The following configurations are possible:

Power-Saving Modes	Watchdog Timer	J3
enabled	disabled	closed*
disabled	enabled	open

*= Default setting

Table 4: J3 Power-Saving Mode / Watchdog Timer Configuration

3.4 J4 Oszillator Watchdog

Upon delivery of the module, the Oscillator Watchdog is not activated, enabling a quick power-on reset of and stable operation of the controller.

The following configurations are possible:

Oszillator Watchdog	J4
enabled	open
disabled	closed*

*= Default setting

Table 5: J4 Oszillator Watchdog Configuration

3.5 J5, J6 First Serial Interface

Jumpers J5 and J6 connect both signals of the controller's serial interface 0 (Serial0) with the RS-232 transceiver of the miniMODUL-537/509 at pins 45(23A) and 47(24A) at X1A. Additionally, a TTL connection is enabled when controller signals are directly connected to pins 15(8A) and 16(8B) of the module (P3.0 and P3.1). At the time of delivery the RS-232 interface is active by default.

The following configurations are possible:

Signal Level First Serial Interface	J5	J6
RS-232 level (module pins 45 und 47)	closed*	closed*
TTL level (module pins 15 und 16)	open	open

*= Default setting

Table 6: J5, J6 First Serial Interface Configuration

3.6 J7, J8 Second Serial Interface

Jumpers J7 and J8 connect both pins of the controller's serial interface 1 (Serial1) with an RS-232 or RS-485 transceiver of the miniMODUL. Likewise, the serial interface 1 signals with their TTL level are directly connected to pins 56(28B) and 57(29A) at X1B (P6.1 and P6.2).

The following configurations are possible:

Signal Level Second Serial Interface	J7	J8
RS-485 level (module pins 95 und 97)	1 + 2*	1 + 2*
RS-232 level (module pins 46 und 55)	2 + 3	2 + 3
TTL level (module pins 120 und 121)	open	open

*= Default setting

Table 7: J7, J8 Second Serial Interface Configuration

3.7 J9, J10, J11 RS-485 Control

Closing Jumper J9 connects the Data-Enable input of the RS-485 transceiver to pin P5.1 of the controller. This allows software-configuration of the RS-485 transmitter for networking purposes.

The following configurations are possible:

RS-485 Transmitter	J9	P5.1	RES
Transmit locked	open	don´t care	don´t care
	closed*	don´t care	high
Transmitter released	closed*	low	low
	closed*	high	don´t care

*= Default setting

Table 8: J9 RS-485 Transmitter Control Configuration

Closing Jumper J10 enables receipt capabilities of the RS-485 transceiver.

The following configurations are possible:

RS-485 Receiver	J10
Receiver locked	open
Receiver released	closed*

*= Default setting

Table 9: J10 RS-485 Receiver Control Configuration

Closing Jumper J11 connects the inverted Data-Output of the RS-485 receiver with pin P3.2 of the controller. As this pin is bit-addressable, Jumper J11 enables bit-addressed commands regarding the status of the data-output.

The following configurations are possible:

Controller Pin P3.2	J11
Disconnected from the inverted data output	open
Connected with the inverted data output	closed*

*= Default setting

Table 10: J11 RS-485 Data Output Configuration

3.8 J12 RS-232 Control

Opening Jumper J12 deactivates the RS-232 transceiver. If this transceiver is deactivated, it is possible to control the transceiver's activities via the RSDIS input of the module (module pin 53(27A) at X1A). Upon delivery of the module, Jumper J12 is closed and, hence, the RS-232 transceiver is activated.

The following configurations are possible:

RS-232-Transceiver	J12	RSDIS
enabled	closed*	not connected
	open	low
disabled	open	not connected
	open	high

*= Default setting

Table 11: J12 RS-232 Control Configuration

3.9 J13 Chip-Enable RTC-72423 (U10B)

Closing Jumper J13 connects the Real-Time-Clock RTC-72423 with the address decoder's pre-decoded Chip Select signal /CS1. Opening Jumper J13 allows the user to connect any desired Chip Select signal via the /CSRTC signal of the module (module pin 59[30A] at X1A).

This jumper remains open at time of delivery due to compatibility reasons with older revisions of the module.

Chip-Enable RTC-72423 (U10B)	J13
externes /CSRTC an Modulpin 59	open*
/CS1 from address decoder	closed

*= Default setting

Table 12: J13 Chip-Enable RTC-72423 Configuration

3.10 J14 Internal Programming Mode on the C509

Jumper J14 is only relevant for modules populated with the Infineon C509 controller. Connecting jumper pads 2+3 enables an optional programming mode for the C509, which can be activated per software. This exchanges XDATA and CODE memory areas and enables an application running from the RAM to program the Flash memory. This is facilitated by a special /WRF signal, which generates writes cycles to the Flash. The design of the board, however, does not utilize this mode for programming the Flash memory. This is done via the FlashTools (refer to the QuickStart Instructions manual). It is recommended that J14 remains closed at position 1+2.

The following configurations are possible:

Programming Mode C509	J14
closed	1 + 2*
opened	2 + 3

*= Default setting

Table 13: J14 C509 Programming Mode Configuration

3.11 J15 E²PROM/FRAM Supply Voltage

The device at U13 can be connected to VCC or VPD using Jumper J15. As default, U13 is populated with a serial E²PROM with voltage supply pins connected to VCC. Alternatively, a serial FRAM device can also populate U13, in order to support frequent write cycles, for instance. If mounted with an FRAM device, the circuit supply pins can be applied to the battery voltage VPD for purposes of data buffering.

The following configurations are possible:

Supply Voltage for U13	J15
E²PROM/FRAM at U13 supplied with VCC	1 + 2*
E²PROM/FRAM at U13 supplied with VPD	2 + 3

*= Default setting

Table 14: J15 E²PROM/FRAM Supply Voltage Configuration

3.12 J16, J17 Address of the Serial E²PROM / FRAM

Jumper J16 and J17 configure the serial E²PROM/FRAM address. The default configuration sets the address to 0xA8.

The following configurations are possible:

Address E²PROM/FRAM	J16	J17
0xA0	1 + 2	2 + 3
0xA4	2 + 3	2 + 3
0xA8	1 + 2*	1 + 2*
0xAC	2 + 3	1 + 2

* = Default setting

Table 15: J16, J17 E²PROM/FRAM Address Configuration

3.13 J18 Write Protection of E²PROM/FRAM

Various types of E²PROM/FRAM can populate space U13. Some of these devices provide a write protection function[1]. Closing Jumper J18 connects pin 7 of the serial E²PROM/FRAM with VCC and thus activates write protection.

The following configurations are possible:

Write Protection E²PROM/FRAM	J18
Write protection of E²PROM/FRAM deactivated	open*
Write protection of E²PROM/FRAM activated	closed

* = Default setting

Table 16: J18 Write Protection of E²PROM/FRAM

3.14 J19 – J22 Using the ICE/Connect

For the use of emulators the controller signals */XXP* can be isolated from the remaining module signals */XX* and can also be connected to an outside source. The relevant signals are /PSEN (J19), /RD (J20), /WR (J21) and /RES (J22). Upon delivery the Jumpers J19-J22 are closed and thus connecting the controller signals to the module signals.

1: *Refer to the corresponding E²PROM/FRAM Data Sheet for more information on the write protection function.*

4 Memory Models

The miniMODUL-537/509 allows for flexible address decoding which can be configured by software to different memory models. A hardware reset activates a default memory configuration that is suitable for a variety of applications. However, this memory model can be changed or adjusted at the beginning of a particular application.

Configuration of the memory is done within the address decoder by means of 4 internal decoder registers: two Control Registers, one Address Register and one Mask Register. All registers are carried out as write-only registers with access through the controller's XDATA memory space. There are two distinct address areas - selectable by means of the bit IO-SW in Control Register 1 - by which the registers can be accessed (*refer to the description of the bit IO-SW below*). Due to a lack of read access, a copy of all register contents should be maintained within your application. Reserved bits may not be changed during the writing of the register; contents must remain at 0. A hardware reset erases all registers while preserving the configuration of the default memory model.

Note:
In the event that you use FlashTools – PHYTEC's proprietary firmware allowing convenient on-board Flash programming - the address FA16 is preset at the start of your application software (*refer to section 4.1, "Control Register 1"*). This is to be noted upon installation of the software copy of the register contents.

The following figure illustrates the default memory model:

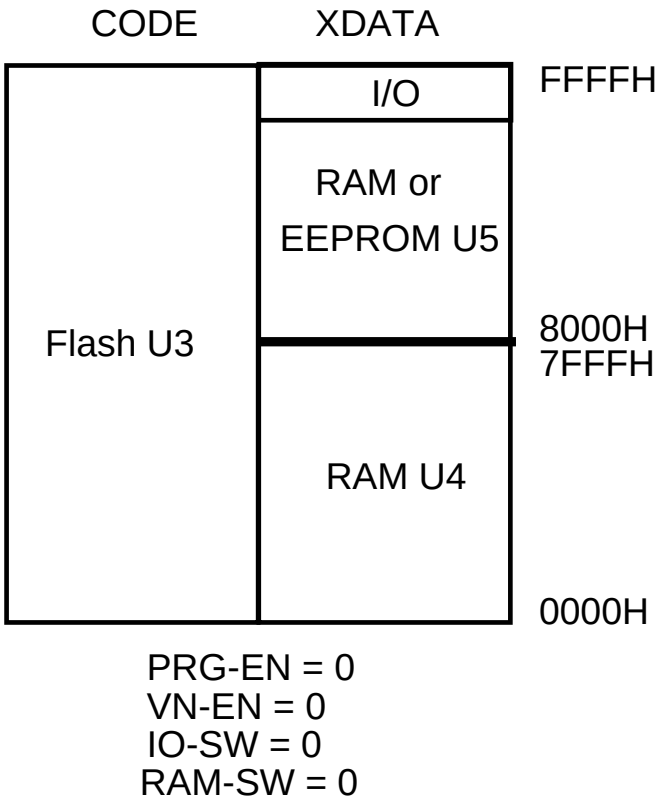


Figure 8: Default Memory Model following a Hardware Reset

It should be noted that the memory block U4 and U5 comprise separate 32 kByte memory areas in the XDATA address area of the controller. In the event that a 128 kByte RAM device is installed at U4, then blocks of 32 kByte can be accessed and switched via bank-latching. In the event that either U4 or U5 is not populated by a memory device, then there is no possible access to the corresponding XDATA memories. The corresponding I/O area is mapped to the XDATA memory space. Within this I/O area; there is no access to any available RAM.

The following sections describe the address decoder's registers for configuration of the memory model.

4.1 Control Register 1

Control Register 1 (Address 7C00H / FC00H)							
Bit 7							Bit 0
PRG-EN	IO-SW	RAM-SW	VN-EN	FA18	FA17	FA16[1]	FA15

Table 17: Control Register 1 of the Address Decoder

Bit invalid in programming model (*refer to PRG-EN*)
Bit valid only in programming model (*refer to PRG-EN*)

PRG-EN: Can be used to activate the special Flash programming memory model (PRG-EN = 1). This model is used within FlashTools[2] for Flash programming purposes and is of limited use within user applications because of its special restrictions.

In this model, 32 kByte Flash memory located within the address range 0000H - 7FFFH is accessible, as well as 32 kByte RAM within the range 8000H - FFFFH. The Flash memory can only be written in the XDATA area and can only be read from the CODE area. The RAM can be read and written in the XDATA area. RAM can also be read from the CODE area. The address line A15 of the Flash is derived from the Control Register 1 (Bit 0, FA15) only in the programming configuration. In the Runtime configuration (PRG-EN = 0), the address line A15 of the controller leads directly to the Flash device.

1: In the event that you use the FlashTools - a firmware allowing convenient on-board Flash-programming - it should be noted that the Bit FA16 will be preset at the start of your application software. This is to be noted upon installation of the software copy of the register contents.

2: The FlashTools firmware is pre-installed in the external Flash device upon delivery of the module.

The bit IO-SW is also relevant to the programming model, whereas the bit VN-EN is not relevant. The following figure illustrates the programming model (the I/O area is not represented):

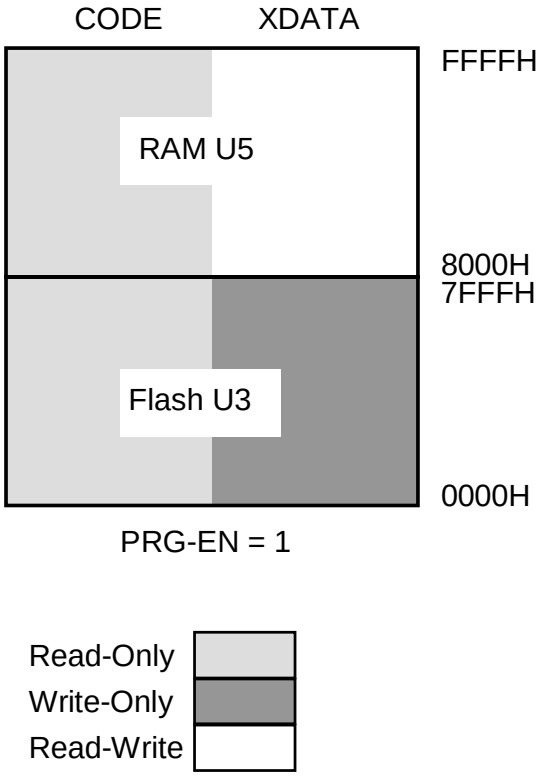


Figure 9: Memory Model for Flash Programming

IO-SW: By means of this bit, the I/O area of the module can be selectively mapped either to the upper or to the lower 32 kByte of the address space. With IO-SW = 0 following a hardware reset, the I/O area is accessible in the range between FC00H - FFFFH. Setting bit IO-SW = 1 maps the I/O area to 7C00H - 7FFFH.

This I/O area generally consists of 4 blocks of 256 bytes each. In three of these blocks, the address decoder provides a pre-decoded Chip Select signal that simplifies the connection of peripheral hardware to the module.

These Chip Select signals will be activated on read/write access to the XDATA memory space within the appropriate address range. The fourth block is reserved for internal access to the decoder's internal register (write-only access). This block is **not** available for use of connecting external devices.

The I/O area configuration is shown in the picture below:

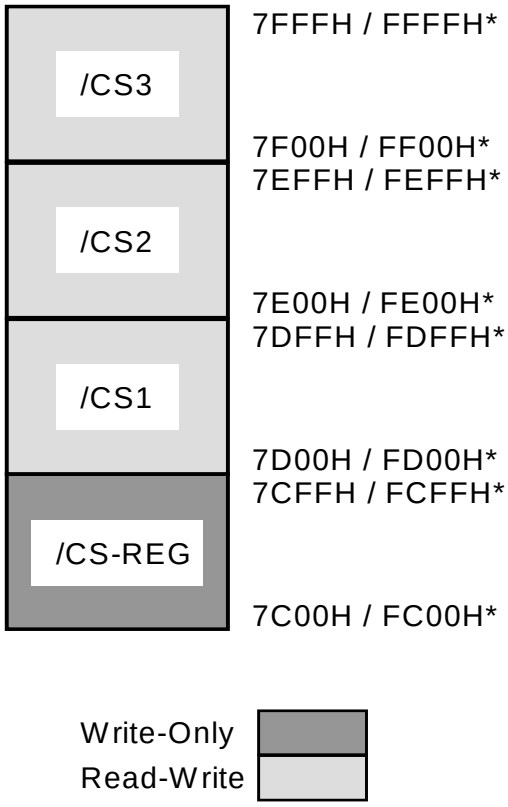


Figure 10: Configuration of the I/O Area

The areas referred to as /CS1 to /CS3 are the freely available Chip Select signals; while the signal /CS-REG is the decoder's internal signal. This latter signal is required to access the internal registers. This signal is not available to the user and no external circuitry should be connected within the address area valid for the /CS-REG signal. In order to ensure proper functioning of FlashTools[1] firmware, enabling on-board programming of the Flash memory, it is essential that the /CS-REG signal be used as described herein. These internal registers are located at address 7C00H - 7C03H (IO-SW = 1) or FC00H - FC03H (IO-SW = 0). The rest of the /CS-REG block remains unused and is reserved for future expansion.

RAM-SW: This bit enables exchange of a 32 kByte memory portion of the RAM devices installed at U4 and U5. Following a hardware reset (RAM-SW = 0) the RAM U4 is mapped in the XDATA address area from 0000H - 7FFFh and RAM/E²PROM at U5 is addressable from 8000H to FFFH. Setting bit RAM-SW = 1 enables access to RAM at U4 in the address area 8000H - FFFFH. Likewise, access to RAM/E²PROM at U5 is possible in the address area 0000H - 7FFFH. In the corresponding I/O areas, there is no access to any memory device.

1: Firmware portion of the utility program for on-board Flash programming and is pre-installed in the Flash at time of delivery.

VN-EN: This bit enables free selection of von Neumann memory[1] within the address space of the controller. Following a hardware reset, the Harvard[2] architecture is configured as default. The von Neumann memory is especially useful when programming code is to be downloaded and subsequently run during runtime, as is the case with a Monitor program. The location of the optional von Neumann memory areas is defined by the Address and Mask Registers (*see below*).

Following a hardware reset (VN-EN = 0), the settings in the Address and Mask Registers are not released. The von Neumann memory is not available at this time. Setting bit VN-EN = 1 activates the Address and Mask Registers and incorporates their settings into access control for von Neumann memory areas. This bit is only relevant in the runtime model (PRG-EN = 0). In the programming model (PRG-EN = 1) bit VN-EN is unimportant and will be ignored.

1: Memory space in which no difference is made between CODE and XDATA access. This means that both accesses use the same physical memory device, usually a RAM.

2: Memory space in which CODE and XDATA accesses use physical different memory devices. CODE access typically uses a ROM or Flash device, whereas XDATA access uses a RAM.

FA[18..15]: The miniMODUL-537/509 can be optionally populated with a Flash device of 512 kByte capacity. Because of the limited 64 kByte address space of the microcontroller, the remainder of the Flash memory can only be accessed by bank switching.

In the runtime model (PRG-EN = 0), 64 kByte banks can be switched by controlling the upper address lines A[18..16] for the Flash through software. For this purpose, register bits FA[18..16] of the address decoder provide a latch to which the desired upper addresses can be written.

Of particular note is the bit FA15, which is solely relevant in the programming model (PRG-EN = 1). As in this model only 32 kByte of Flash can be accessed, it serves as address line A15 for the Flash memory. In the runtime model (PRG-EN = 0) with a 64 kByte Flash memory area, to contrast, the address line A15 of the controller is attached directly to the Flash.

The function of the bits FA[18..16] depends on the hardware configuration of the module. As described above, these bits are only relevant if the miniMODUl-537/509 is populated with a Flash device of 512 kByte capacity.

4.2 Control Register 2

Control Register 2 (Address 7C01H / FC01H)							
Bit 7							Bit 0
N/A[1]	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	RA16	RA15

Table 18: Control Register 2 of the Address Decoder

RA16: The module can optionally accommodate a 128 kByte RAM device at U4. As the address space at U4 is limited to 32 kByte in the XDATA area of the controller, the remainder of the RAM can only be accessed by bank switching.

Four memory banks of 32 kByte banks can be switched by setting the high address-lines A[16..15] through software. For this purpose, register bit RA[16..15] of the address decoder provides a latch to which the desired upper addresses can be written.

The function of this bit is dependent on the hardware configuration of the module and functions, as described above, only in connection with RAM devices of at least 128 kByte at U4.

[1]: N/A: Not Accessible

4.3 Address Register

The Address Register 7C02H / FC02H functions in conjunction with the Mask Register (*see section 4.4*) to define the von Neumann[1] and Harvard[2] memory area in the controller's memory space. By setting the bit VN-EN in Control Register 1, the values of the Address and the Mask Register become valid for the definition of von Neumann and Harvard memory areas and will be incorporated in address decoding. (*refer to section 4.1, "Control Register 1"*)

The location of one or more Harvard memory areas can be configured with both registers. The remaining areas of the memory space are configured as von Neumann memory in which RAM is accessible in both XDATA and CODE memory space.

The mechanism for the memory space distinction is based on a comparison of the current address with a pre-defined address pattern of variable width. If the relevant bit positions of the address matches the pre-defined address pattern, memory access occurs according to the Harvard architecture. If the current address is different to the pre-defined address pattern, memory access occurs according to the von Neumann architecture.

Address Register (Address 7C02H / FC02H)							
Bit 7							Bit 0
HA15	HA14	HA13	HA12	HA11	HA10	*Res.*[3]	*Res.*

Table 19: Address Register of the Address Decoder

1: Memory space in which no difference exists between CODE and XDATA access. This means that both accesses use the same physical memory device, usually a RAM.

2: Memory space in which CODE and XDATA accesses use different physical memory devices, usually CODE access uses a ROM or Flash device, whereas XDATA access uses a RAM.

3: Reserved bits are not to be changed, the default value (0) must remain.

The Address Register holds the address pattern mentioned above. Each bit of the pattern is compared with the corresponding address line of the controller (HA15 with A15, ..., HA10 with A10). As address lines A15 .. A10 are used to define Harvard memory space, only Harvard areas of at least 1 kByte can be configured. Memory areas smaller than 1 kByte can not be configured.

4.4 Mask Register

The Mask Register (7C03H / FC03H) can be used to mask single bits in the Address Register (*see above*). Following a hardware reset, all bits within the Address Register are relevant. By setting the individual bits in the Mask Register, all corresponding bits in the Address Register will no longer be regarded in the address comparison.

Mask Register (Address 7C03H / FC03H)							
Bit 7							Bit 0
MA15	MA14	MA13	MA12	MA11	MA10	*Res.*[1]	*Res.*

Table 20: Mask Register of the Address Decoder

It is to be noted that in the case of a single 32 kByte RAM, the memory area is mirrored within the controller's addressing area. On account of the insufficient utilization of A15 in this configuration, memory accesses to addresses higher than 8000H are reduced to accesses to the memory area from 0000H to 7FFFH. This should be taken into consideration when choosing the memory model. Otherwise, functional problems could result from overlapping access.

1: Reserved bits are not to be changed, the default value (0) must remain.

The following examples of different combinations of the address- and mask registers illustrate these functions (X=specific bit irrelevant):

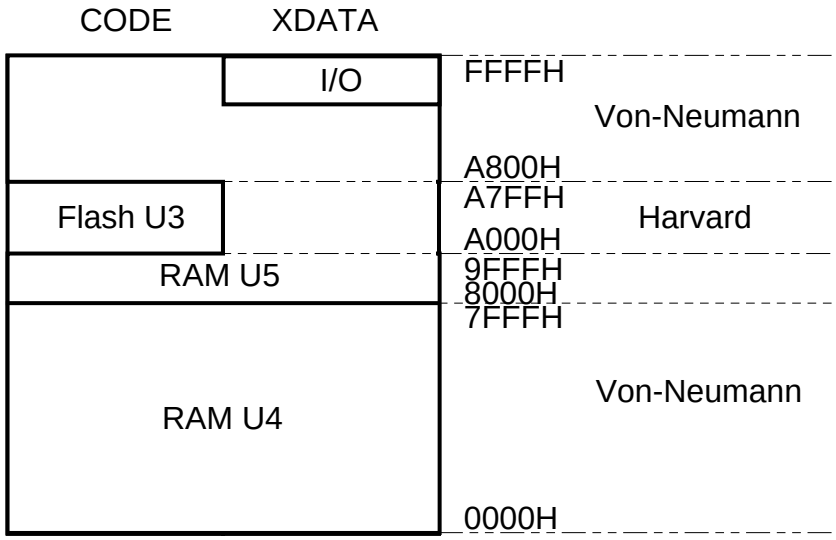
Address Reg.	Mask Reg.	Comments (only for VN-EN = 1)	
1XXXXX00b	01111100b	Harvard von Neumann	8000H-FFFFH, 0000H-7FFFH
0XXXXX00b	01111100b	Harvard von Neumann	0000H-7FFFH, 8000H-FFFFH
11111100b	00000000b	Harvard von Neumann	FC00H-FFFFH, 0000H-FBFFH
010X0000b	00010000b	Harvard and von Neumann and	4000H-43FFH 5000H-53FFH, 0000H-3FFFH, 4400H-4FFFH 5400H-FFFFH
10000000b	00000000b	Harvard von Neumann and	8000H-83FFH, 0000H-7FFFH 8400H-FFFFH
10100X00b	00000100b	Harvard von Neumann and	A000H-A7FFH, 0000H-9FFFH A800H-FFFFH

Table 21: Example of Address Decoder Functions

Reserved bits without function for address decoding (*refer to description of the register*).

X = irrelevant (on account of a bit set in the Mask Register)

The last example from the above table is further illustrated by the following figure:



PRG-EN = 0
VN-EN = 1
IO-SW = 0
RAM-SW = 0
Adr.-Reg. = 10100X00b
Mask.-Reg. = 00000100b

Figure 11: Example of a Memory Model

5 Flash Memory

Flash, as non-volatile memory on the miniMODUL-537/509, provides an easily reprogrammable means of code storage to the user. The miniMODUL-537/509 can be populated at U3 by a single Flash device of type 29F010 with two banks of 64 kByte each or device type 29F040 with 8 banks of 64 kByte each.

Flash memory devices offer up to 100,000 reprogramming cycles, and enable on-board programming of user code. These Flash devices are programmable with 5 V. No dedicated programming voltage is required. All standard versions of the miniMODUL-537/509 feature a programming utility firmware – FlashTools (*refer to applicable QuickStart Instruction for more details*) – resident in the Flash device.

This firmware enables on-board download, as well as subsequent erasure and reprogramming, of user code into the Flash with the help of an intuitive PC-side software. The FlashTools firmware portion resides in the initial 32 kByte of Flash memory, which is not available for storage of user code. The total memory available for user programs is 64 kByte (29F010) or 448 kByte (29F040) *(refer to Figure 12)*.

Note:
Should the FlashTools firmware portion be erased from the Flash device without having a back-up or an equivalent replacement, reprogramming is no longer possible!

Please note that this firmware protects itself against any intentional or accidental erasure or overwriting. As the Flash device's hardware protection mechanism is not utilized, protection is limited to the software level. In the event that a user wishes to download his or her own programming algorithms or tools into the Flash, the user must ensure that a programming tool remains in the Flash memory. *Refer to the "QuickStart Instructions" for a detailed description of the on-board programming procedure.*

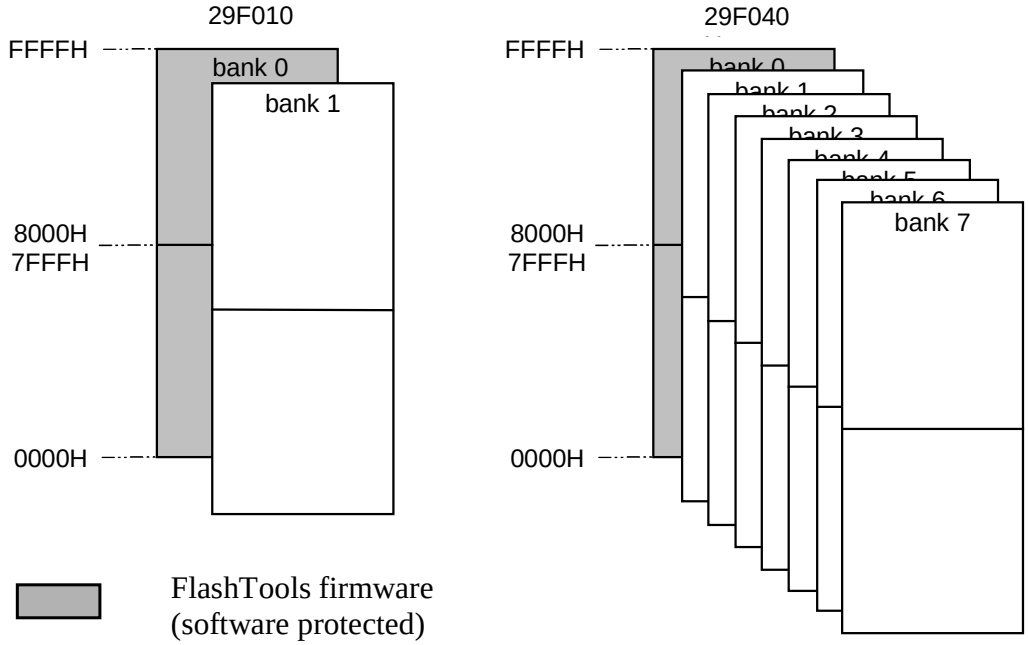


Figure 12: Memory Areas of the Flash Device

Use of a Flash device as the only code memory results in limited usability of the Flash as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash's internal programming process, the reading of data from Flash is not possible. For Flash programming, program execution must be transferred out of Flash (such as into von Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100.000 erase/program cycles.

6 Battery Buffer

The battery that buffers the memory is not essential to the functioning of the miniMODUL-537/509. However, this battery buffer embodies an economical and practical means of storing nonvolatile data in SRAM and is necessary for data storage in the Real-Time Clock in case of a power failure.

The VBAT input (pin 42(21B) at X1A) is provided for connecting the external battery. The negative polarity pin on the battery must connect to GND on the miniMODUL-537/509. As of the printing of this manual, a lithium battery is recommended as it offers relatively high capacity at low discharge. In the event of a power failure at VCC, the SRAMs and the RTC will be buffered by a battery connected to VBAT.

Power consumption depends on the components used and memory area. *Refer to corresponding Data Sheets for the RAM devices mounted on the board* (*refer also to section 9,"Technical Specifications").* This is typically < 1 µA per 32 kByte RAM device installed on the miniMODUL.

Note:
If an E²PROM device populates the miniMODUL-537/509 at U5 we do not recommend using the battery buffer. Therefore Jumper J2 has to be closed at position 1+2 in order to avoid fast discharge of the battery.
Be advised that despite the battery buffer, changes in the data content within the RAM can occur. The battery buffer does not completely remove the danger of data destruction.

7 Real-Time Clock RTC-8564 (U12)

For real-time or time-driven applications the miniMODUL-537/509 is equipped with an RTC-8564 Real-Time Clock (RTC) at U12. This RTC device provides the following features:

- serial input/output bus (I^2C)
- power consumption
  bus active: max. 50 mA
  bus inactive, CLKOUT = 32 kHz : max. 1.7 µA
  bus inactive, CLKOUT = 0 kHz : max. 0.75 µA
- clock function with four year calendar
- century bit for year 2000 compliance
- universal timer with alarm and overflow indication
- 24-hour format
- automatic word address incrementing
- programmable alarm, timer and interrupt functions

If the miniMODUL-537/509 is equipped with a battery, the Real-Time Clock runs independently of the module's power supply.

Programming of the Real-Time Clock is done via the I^2C bus (I^2C address 0xA2 = 10100010), connected to port P6.4 (SCL) and port P6.5 (SDA) on the controller. The Real-Time Clock also provides an interrupt output which extends to header pin X1A30B (60). An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. All interrupts must then be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet located on the Spectrum CD.*

Note:
Following attachment of a power supply to the board, the RTC-8564 generates **no** interrupts, as the RTC is not yet initialized.

8 Serial E²PROM/FRAM (U13)

A non-volatile memory with a serial (I²C bus) interface populates space U13 on the miniMODUL-537/509. This device is intended to store configuration parameters and user data. This memory device can be in the form of an E²PROM device or an FRAM device. The I²C bus is generated using port pins P6.4 (SCL) and port P6.5 (SDA).

A description of the I²C memory protocol of the specific memory component at U13 can be found in the respective Data Sheet.

Table 22 gives an overview of the memory components that can be used at U13 at the time of printing of this manual.

Device Type	Manufacturer	Size	Component
E²PROM	Microchip	32 kByte	MIC24LC256
	Catalyst	4 kByte*	CAT24WC32
		8 kByte	CAT24WC64
	ST	4 kByte*	M24C32
		8 kByte	M24C64
FRAM	Ramtron	512 Byte	FM24C04
		8 kByte	FM24C64

* = Default size

Table 22: Memory Device Options for U13

Various available E²PROM/FRAM types provide a write protection function[1]. Jumper J18 is used to activate this function. If this jumper is closed, then pin 7 of the serial E²PROM/FRAM is connected to VCC.

Write Protection E²PROM/FRAM	J18
Write protection of E²PROM/FRAM deactivated	open*
Write protection of E²PROM/FRAM activated	closed

* = Default setting

Table 23: E²PROM/FRAM Write Protection

[1]: *Refer to the corresponding E²PROM/FRAM Data Sheet for more information on the write protection function.*

Jumper J16 and J17 configure the address of the serial E²PROM/FRAM. The default configuration sets the address to 0xA8.

E²PROM/FRAM Address	**J16**	**J17**
0xA0	1 + 2	2 + 3
0xA4	2 + 3	2 + 3
0xA8	1 + 2*	1 + 2*
0xAC	2 + 3	1 + 2

* = Default setting

Table 24: E²PROM/FRAM Address

9 Technical Specifications

The physical dimensions of the miniMODUL-537/509 are represented in *Figure 13*. The module's profile is ca. 10 mm thick, with a maximum component height of 3 mm on the back-side of the PCB and approximately 5 mm on the front-side. The board itself is approximately 1.5 mm thick.

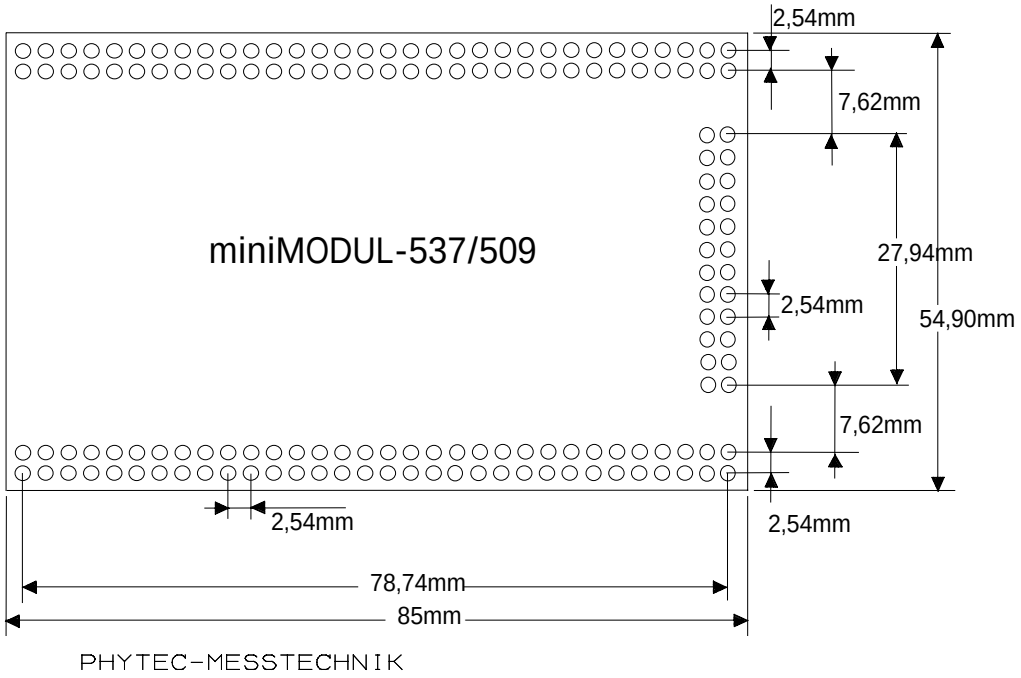


Figure 13: Physical Dimensions

Additional specifications:

- Dimensions: 54.9 x 85 mm, ±0,01 mm
- Weight: approximately 44 grams with 160 kByte RAM device, socketed 128 kByte Flash device, approximately 32 grams with standard configuration, 32 kByte RAM without socket
- Storage temperature: -40°C to +90°C
- Operating temperature: standard 0°C to +70°C, extended -40°C to +85°C
- Humidity: maximum 95 % r.F. not condensed
- Operating voltage: 5 V ±5 %, VBAT 3 V ±20 %
- Power consumption: maximum 140 mA, typ. 100 mA at 12 MHz oscillator frequency and 128 kByte RAM at +20°C
- Power consumption with battery buffer: maximum 10 µA per RAM device, typically 1 µA per RAM device at +20°C

These specifications describe the standard configuration of the miniMODUL-537/509 as of the printing of this manual.

Caution:
Please note that the module storage temperature is only 0°C to +70°C if a battery buffer is used for the RAM devices.

10 Hints for Handling the Module

When changing controllers please ensure that appropriate PLCC extraction tools are used and that the socket and all components remain free from intrusive damage. It is also advisable to ensure that all insertable controllers are pin-compatible with the 80C32, and that all special hardware features are compatible with the layout of the board.

Removal or exchange of components on the miniMODUL-537/509 (controller, memory, quartz etc.) is not advisable given the compact nature of the miniMODUL-537/509. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged during removal. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighbouring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Index

Document: **miniMODUL-537/509**
Document number: **L-627e_3, February 2003**

How would you improve this manual?

Did you find any mistakes in this manual? page

Submitted by:
Customer number: _____

Name: _____

Company: _____

Address: _____

_____

Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

Published by PHYTEC

Ordering No. L-627e_3
Printed in Germany