phyCARD-S

Preliminary

HARDWARE MANUAL

EDITION JULY 2009

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	EUROPE	NORTH AMERICA
Address:	PHYTEC Technologie Holding AG Robert-Koch-Str. 39 D-55129 Mainz GERMANY	PHYTEC America LLC 203 Parfitt Way SW, Suite G100 Bainbridge Island, WA 98110 USA
Ordering Information:	+49 (800) 0749832 order@phytec.de	1 (800) 278-9913 sales@phytec.com
Technical Support:	+49 (6131) 9221-31 support@phytec.de	1 (800) 278-9913 support@phytec.com
Fax:	+49 (6131) 9221-33	1 (206) 780-9135
Web Site:	http://www.phytec.de	http://www.phytec.com

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1 Preface

This hardware manual describes the phyCARD-S Single Board Computer's design and function. Precise specifications for the Freescale i.MX27 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

In this hardware manual and in the attached schematics, active low signals are denoted by a "/" or "#" preceding the signal name (e.g.: /RD or #RD). A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCARD-S

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCARD-S is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCARD OEM modules, which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1.1 Introduction

The phyCARD-S belongs to PHYTEC's phyCARD Single Board Computer module family. The phyCARD SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCARD boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCARD board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCARD boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCARD boards even in high noise environments.

phyCARD boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCARD users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCARD-S is a subminiature (60 x 60 mm) insert-ready Single Board Computer populated with the Freescale i.MX27 microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connector aligning one sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or datasheet. The descriptions in this manual are based on the Freescale i.MX27. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCARD-i.MX27.

The phyCARD-S offers the following features:

- Subminiature Single Board Computer (´60 x 60 mm) achieved through modern SMD technology
- Populated with the Freescale i.MX27 microcontroller (BGA404 packaging)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to one 100-pin high-density (0.635 mm) Molex connectors aligning one sides of the board, enabling it to be plugged like a "big chip" into target application
- Max. 400 MHz core clock frequency
- Boot from NAND Flash
- 64 MByte (up to 1 GByte) on-board NAND Flash[1]
- 32 MByte (up to 512 MByte) Mobile DDR SDRAM on-board
- UART with data rates of up to 460kbps
- 4KB (up to 32kB) I^2C EEPROM
- High-Speed USB OTG transceiver
- Auto FDX/MDX 100MBit Ethernet Controller
- All controller required supplies generated on board
- 4 Channel LVDS (18Bit) LCD-Interface
- Support of standard 20 pin debug interface through JTAG connector
- One I^2C interfaces
- SD/MMC card interface with DMA
- SSI Interface (AC97)
- Optional LVDS Camera Interface

[1] Please contact PHYTEC for more information about additional module configurations.

1.2 Block Diagram

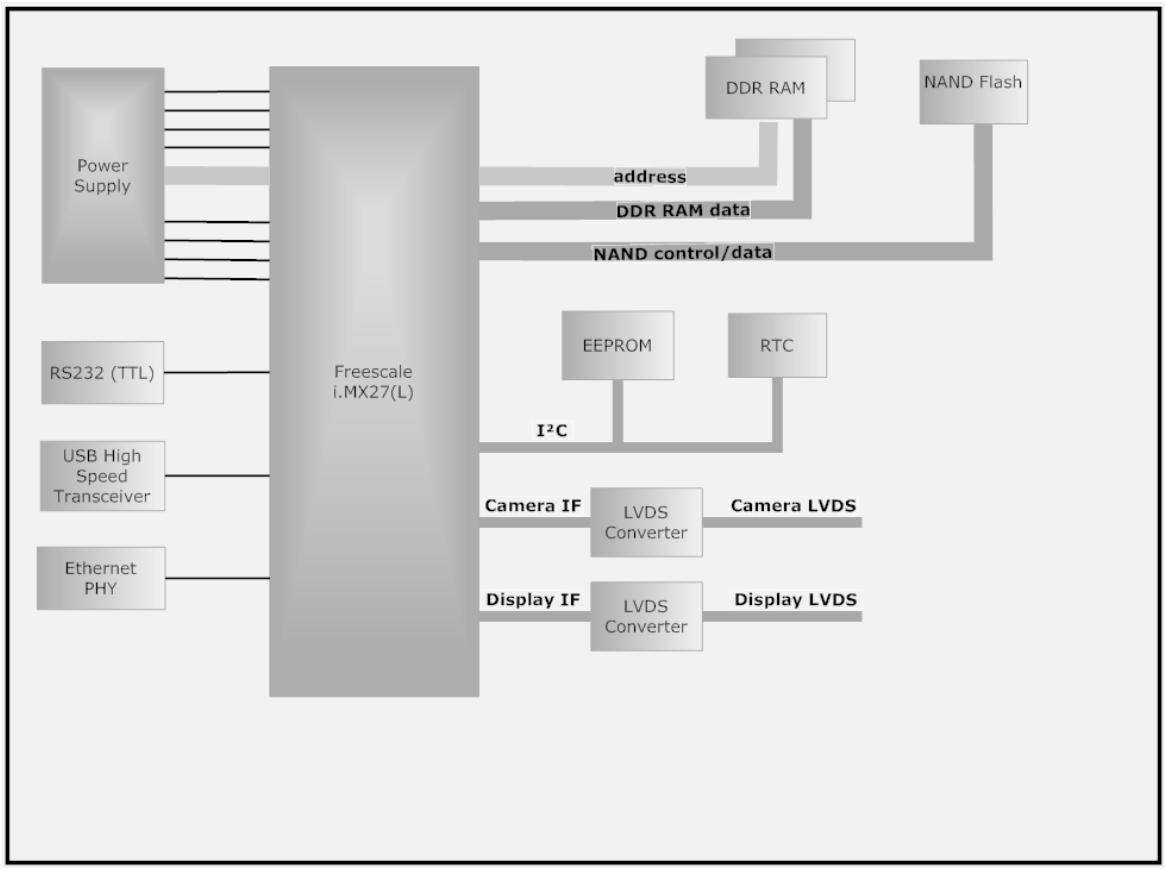


Figure 1: Block Diagram of the phyCARD-S

1.3 View of the phyCARD-S

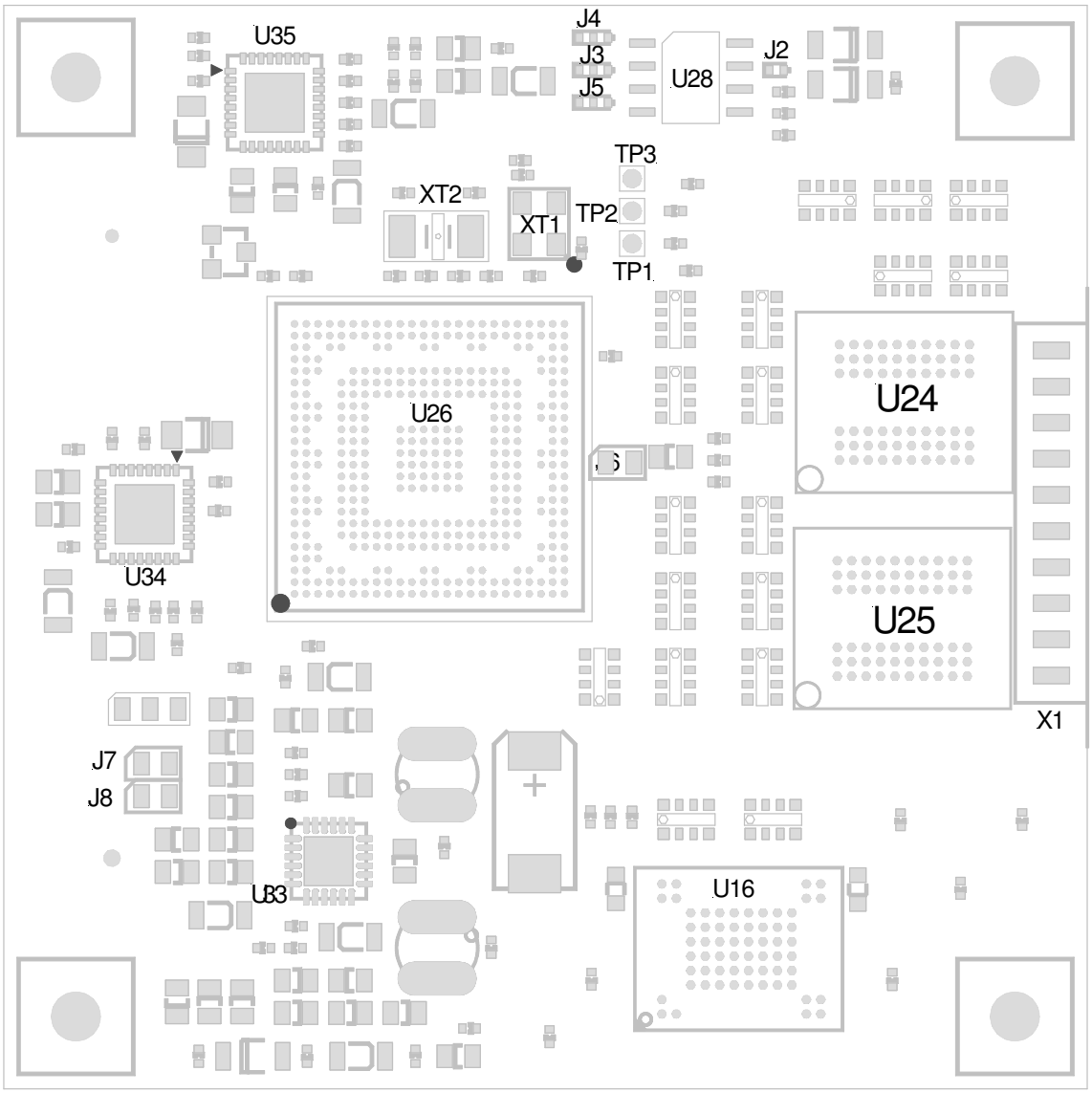


Figure 2: Top view of the phyCARD-S (controller side)

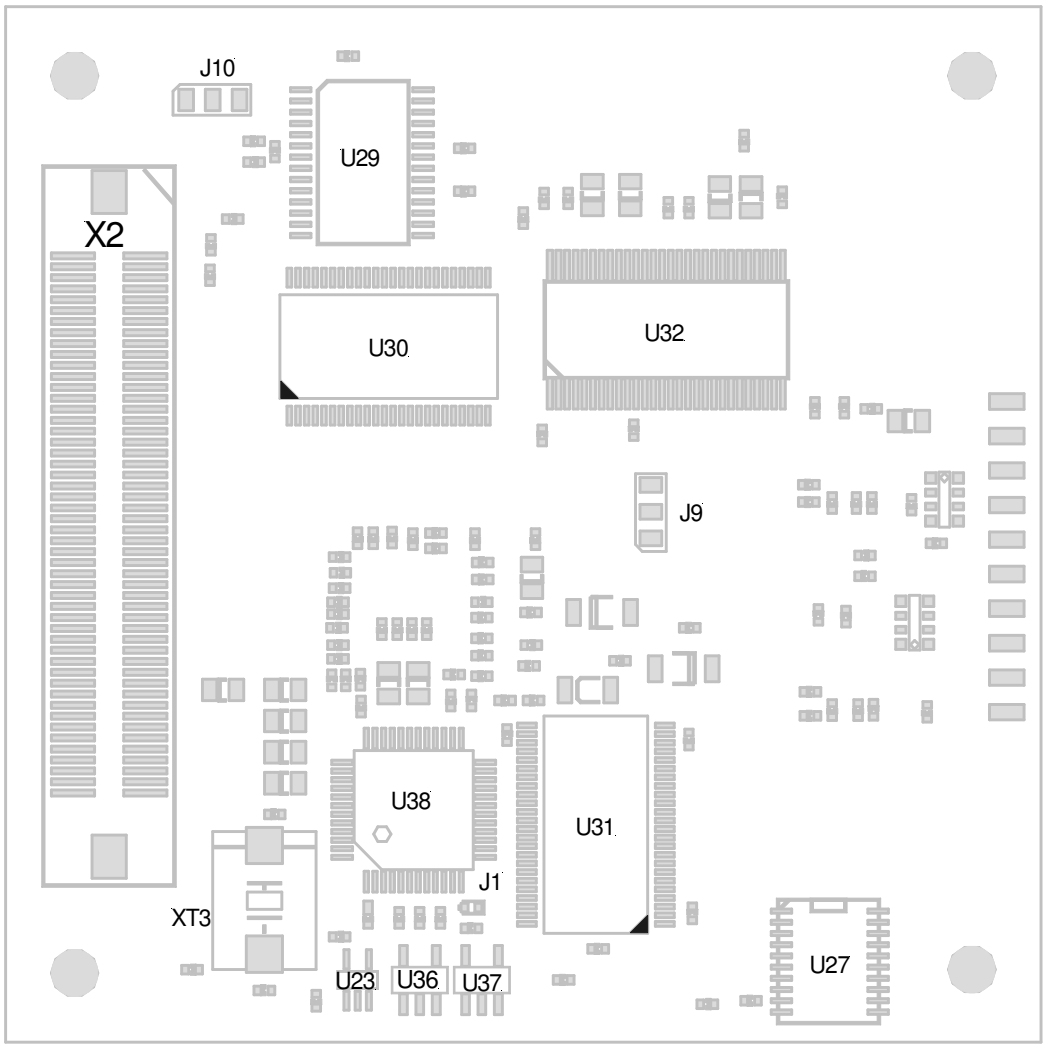


Figure 3: Bottom view of the phyCARD-S (connector side)

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining on side of the module (referred to as phyCARD-connector). This allows the phyCARD-S to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCARD-connector has been introduced with the phyCARD specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCARD-module with the phyCARD-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCARD-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCARD-S (viewed from above; phyCARD-connector pointing down) or with the socket of the corresponding phyCARD Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCARD-S marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module’s phyCARD-connector as well as mating connectors on the phyBASE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCARD-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCARD-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCARD-S with SMT phyCARD-connectors on its underside (defined as dotted lines) mounted on a Development Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCARD-module showing these phyCARD-connectors mounted on the underside of the module’s PCB.

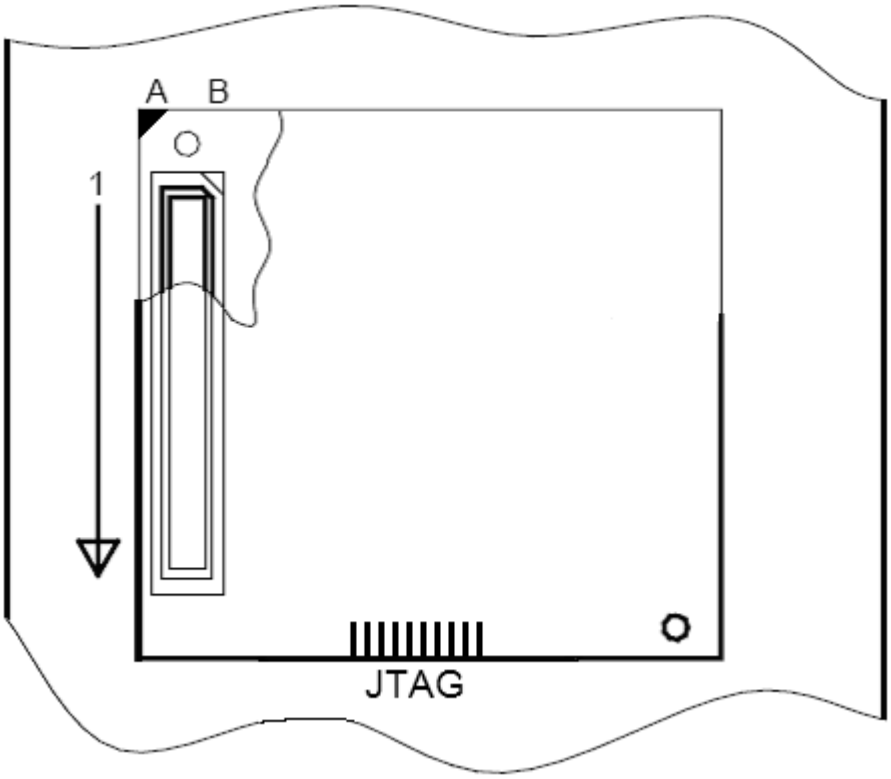


Figure 4: Pin-out of the phyCARD-Connector (top view, with cross section insert)

Table 1 provides an overview of the pin-out of the phyCARD-connector, as well as descriptions of possible alternative functions. Table 1 also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column. The Freescale i.MX27 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. *Please refer to the Freescale i.MX27 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

Note: SL is short for Signal Level (V) and is the applicable logic level to interface a given pin. Those pins marked as "N/A" have a range of applicable values that constitute proper operation.

Table 1: Pin-out of the phyCARD-Connector X1

PIN ROW X1A				
PIN #	**SIGNAL**	**I/O**	**SL**	**DESCRIPTION**
1A	VCC3V3	-	Power	Main Power Input (3,3V)
2A	VCC3V3	-	Power	Main Power Input (3,3V)
3A	VCC3V3	-	Power	Main Power Input (3,3V)
4A	GND	-	-	Ground 0V
5A	VCC_LOGIC	O	VCC_LOGIC	VCC Logic
6A	VCC_FEEDBACK	-	Power	Veeback for VCC3V3
7A	X_#RESET	-	VCC3V3	Active low Reset In
8A	GND	-	-	Ground 0V
9A	TXOUT0+	O	LVDS	LVDS Chanel 0 positive Output
10A	TXOUT0-	O	LVDS	LVDS Chanel 0 negative Output
11A	TXOUT2+	O	LVDS	LVDS Chanel 2 positive Output
12A	TXOUT2-	O	LVDS	LVDS Chanel 2 negative Output
13A	GND	-	-	Ground 0V
14A	TXCLKOUT+	O	LVDS	LVDS Clock positiv Output
15A	TXCLKOUT-	O	LVDS	LVDS Clock negative output
16A	X_CSI_MCLK	O	VCC_LOGIC	Clock Output for Camera Interface
17A	X_I2C_CLK	O	VCC_LOGIC	I2C Clock Output
18A	GND	-	-	Ground 0V
19A	X_ETH_SPPED	O	VCC3V3	Ethernet Speed Indicator (Open Drain)
20A	X_ETH_TX+	O	VCC3V3	Transmit positive output (normal) Receive positive input (reversed)
21A	X_ETH_TX-	O	VCC3V3	Transmit negative output (normal) Receive negative input (reversed)
22A	GND	-	-	Ground 0V
23A	X_USB_HS_/PSW	O	VCC3V3	USB-OTG Power switch output open drain
24A	X_USB_HS_FAULT	I	VCC3V3	USB-OTG over current input signal
25A	GND	-	0	Ground 0V
26A	X_VBUS	I	5V	USB VBUS Voltage
27A	X_UDM	I/O		USB transceiver cable interface, D-
28A	X_UDP	I/O		USB transceiver cable interface, D+
29A	X_UID	I		USB on the go transceiver cable ID resistor connection
30A	GND	-	0	Ground 0V
31A	X_SD2_D0	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode

32A	X_SD2_D2	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
33A	X_SD2_CLK	O	VCC_LOGIC	SD/MMC Clock for MMC/SD/SDIO
34A	GND	-	-	Ground 0V
35A	X_CSPI1_SS0	O	VCC_LOGIC	SPI 1 Chip select 0
36A	X_#CSPI1_RDY	O	VCC_LOGIC	SPI 1 SPI data ready in Master mode
37A	X_CSPI1_SCLK	O	VCC_LOGIC	SPI 1 clock
38A	GND	-	-	Ground 0V
39A	X_UART1_TXD	O	VCC_LOGIC	Serial transmit signal UART 1
40A	X_UART1_RTS	O	VCC_LOGIC	Request to send UART 1
41A	GND	-	-	Ground 0V
42A	Not connected	-	-	Pin left unconnected
43A	SSI1_TXDAT	O	VCC_LOGIC	AC97 Transmit Output
44A	SSI1_RXDAT	I	VCC_LOGIC	AC97 Receive Input
45A	GND	-	-	Ground 0V
46A	GPIO0_IRQ	I/O	VCC_LOGIC	GPIO
47A	GPIO2_IRQ	I/O	VCC_LOGIC	GPIO
48A	Not connected	-	-	Pin left unconnected
49A	GND	-	-	Ground 0V
50A	X_BOOT1	I	-	Boot-Mode 1

PIN ROW X1B				
PIN #	**SIGNAL**	**I/O**	**SL**	**DESCRIPTION**
1B	VCC3V3	-	Power	Main Power Input (3,3V)
2B	VCC3V3	-	Power	Main Power Input (3,3V)
3B	VCC3V3	-	Power	Main Power Input (3,3V)
4B	GND	-	-	Ground 0V
5B	VCC_LOGIC	O	VCC_LOGIC	Display vertical synchronization pulse
6B	VBAT	-	Power	Battery Power Input
7B	X_#RESET_OUT	-	VCC_LOGIC	Active low Reset output
8B	GND	-	-	Ground 0V
9B	TXOUT1+	O	LVDS	LVDS Chanel 0 positive Output
10B	TXOUT1-	O	LVDS	LVDS Chanel 0 negative Output
11B	TXOUT3+	O	LVDS	LVDS Chanel 3 positive Output
12B	TXOUT3-	O	LVDS	LVDS Chanel 3 negative Output
13B	GND	-	-	Ground 0V
14B	RXIN+	O	LVDS	LVDS Receive positiv Input for Camera
15B	RXIN-	O	LVDS	LVDS Receive negativ Input for Camera
16B	LOCK	O	VCC_LOGIC	Lock Output for Camera Interface
17B	X_I2C_DATA	I/O	VCC_LOGIC	I2C Data
18B	GND	-	-	Ground 0V
19B	X_ETH_LINK	O	VCC3V3	Ethernet Speed Indicator (Open Drain)
20B	X_ETH_RX+	O	VCC3V3	Receive positive input (normal) Transmit positive output (reversed)
21B	X_ETH_RX-	O	VCC3V3	Receive negative input (normal) Transmit negative output (reversed)
22B	GND	-	-	Ground 0V
23B	X_USB_HS_/PSW2	O	VCC_LOGIC	USB-HOST Power switch output open drain
24B	X_USB_HS_FAULT 2	I	VCC_LOGIC	USB-HOST over current input signal
25B	GND	-	-	Ground 0V
26B	X_VBUS2	I	5V	USB HOST VBUS Voltage
27B	X_UDM2	I/O		USB HOST transceiver cable interface, D-
28B	X_UDP2	I/O		USB HOST transceiver cable interface, D+
29B	X_UID2	I		USB HOST transceiver cable ID resistor connection
30B	GND	-	-	Ground 0V
31B	X_SD2_D1	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
32B	X_SD2_D3	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
33B	X_SD2_CMD	O	VCC_LOGIC	SD/MMC Command for MMC/SD/SDIO
34B	GND	-	-	Ground 0V

35B	X_CSPI1_SS1	O	VCC_LOGIC	SPI 1 Chip select 1
36B	X_#CSPI1_MOSI	I/O	VCC_LOGIC	SPI 1 Master data out; slave data in
37B	X_CSPI1_MISO	I/O	VCC_LOGIC	SPI 1 Master data in; slave data out
38B	GND	-	-	Ground 0V
39B	X_UART1_RXD	I	VCC_LOGIC	Serial data receive signal UART 1
40B	X_UART1_CTS	I	VCC_LOGIC	Clear to send UART 1
41B	GND	-	-	Ground 0V
42B	SSI1_CLK	-	VCC_LOGIC	AC97 Clock
43B	SSI1_FS	O	VCC_LOGIC	AC97 SYNC
44B	Not connected	-	-	Pin left unconnected
45B	GND	-	-	Ground 0V
46B	X_CSPI1_CD	I	VCC_LOGIC	SPI 1 Card Detect
47B	GPIO1_IRQ	I/O	VCC_LOGIC	Pin left unconnected
48B	Not connected	-	-	Pin left unconnected
49B	GND	-	-	Ground 0V
50B	Not connected	-	-	Pin left unconnected

3 Jumpers

For configuration purposes, the phyCARD-S has 10 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. 7 solder jumpers are located on the top side of the module (opposite side of connectors) and 3 solder jumpers are located on the bottom side of the module (connector side). Table 2 below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

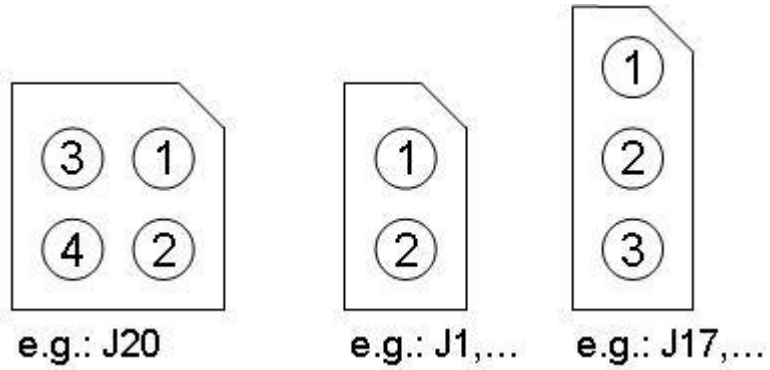


Figure 5: Typical jumper pad numbering scheme

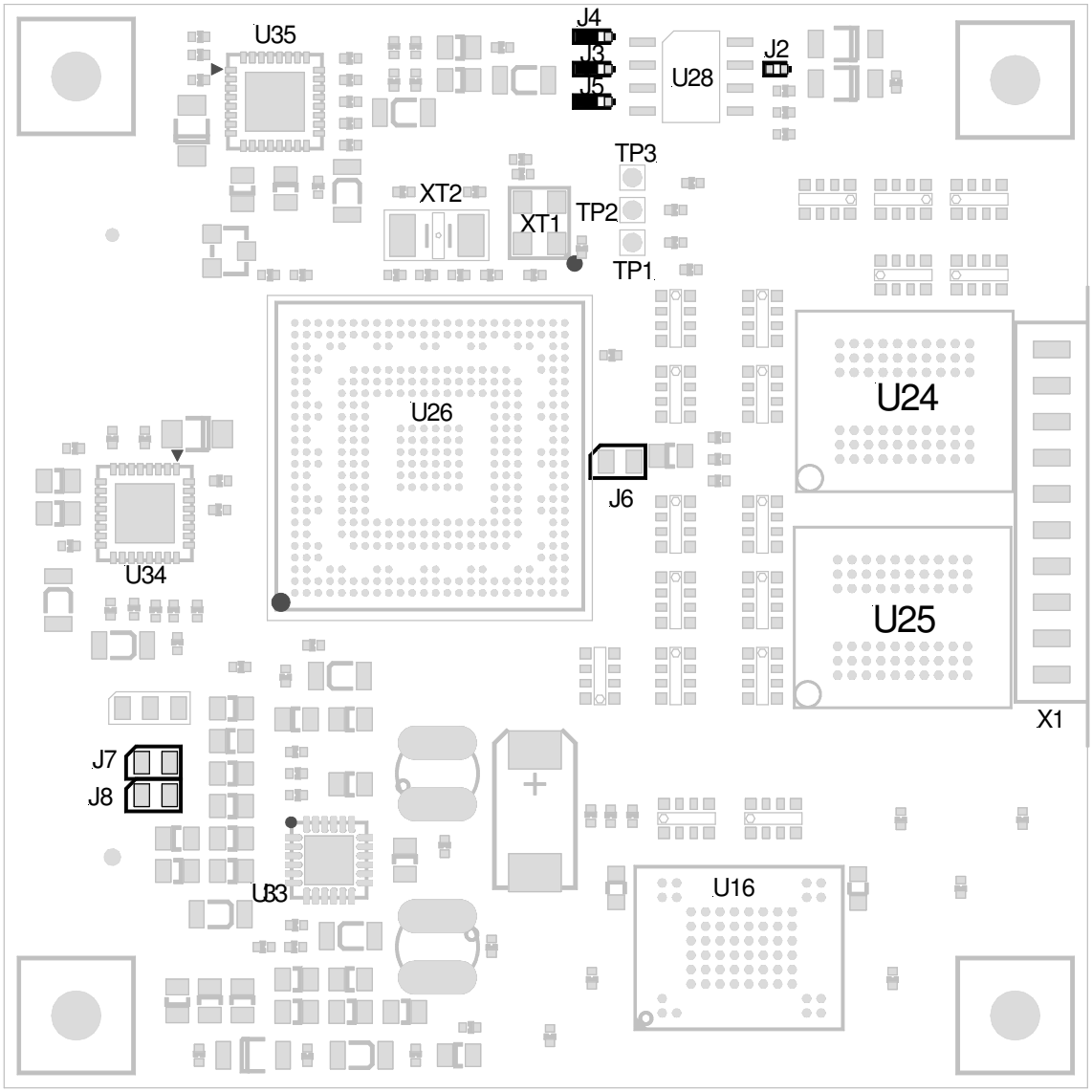


Figure 6: Jumper locations (top view)

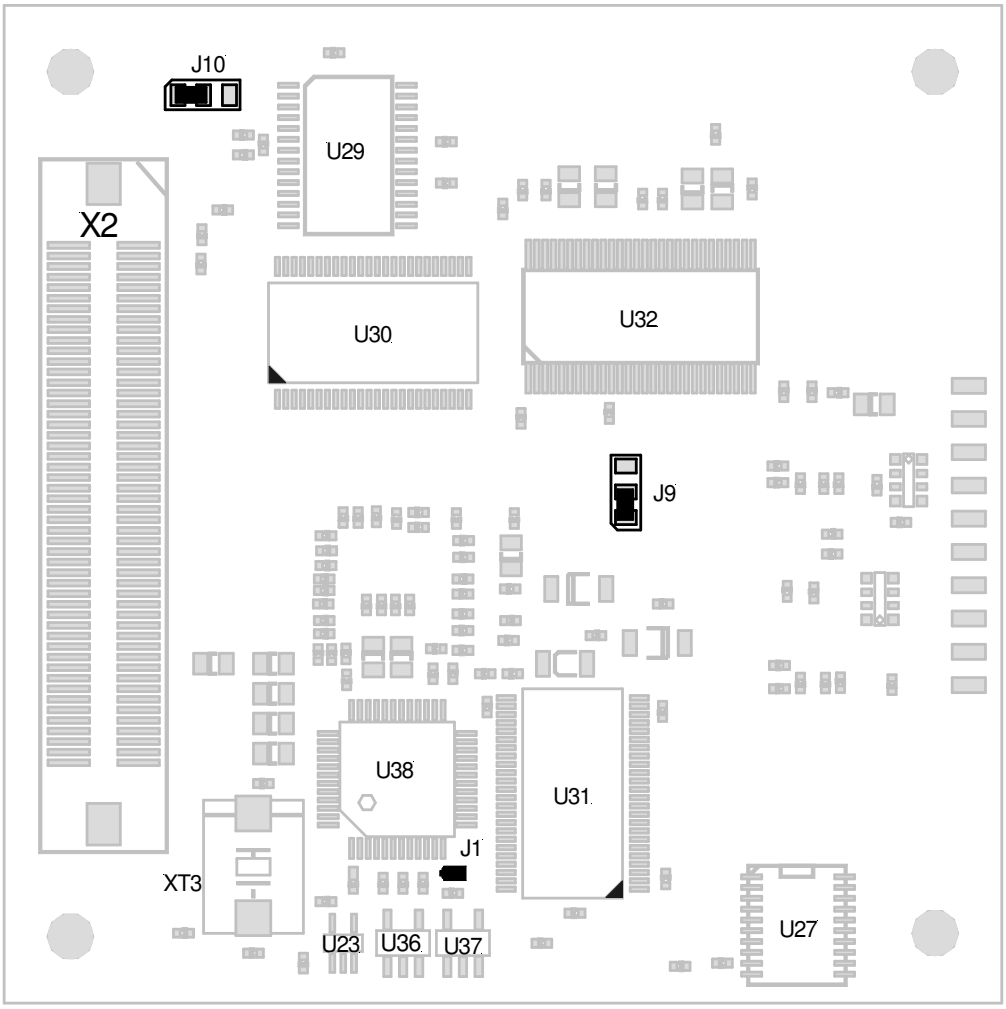


Figure 7: Jumper locations (bottom view)

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper settings

	Default Setting		Alternative Setting		See Section
J1	closed	PC30 is connected with Ethernet Phy Reset	open	PC30 is not connected with Ethernet Phy Reset	
J2	open	EEPROM U28 is not write protected	closed	EEPROM U28 is write protected	
J3	2+3	EEA1 high	1+2	EEA1 low	
J4	2+3	EEA0 low	1+2	EEA0 high	
J5	2+3	EEA2 low	1+2	EEA2 high	
J6	open	VDD_FUSE not connected	closed	VDD_FUSE conneted with VCC3V3. **Attention! Do not close without an order**.	
J7	open	Feedback not used	R1		
J8	open	Feeback not used	R2		
J9	2+3	negative Clock for LVDS	1+2	positive Clock for LVDS	
J10	2+3	negative Clock for CAM	1+2	positive Clock for CAM	

4 Power Requirements

The phyCARD-S normally operates with one voltage supplies denoted as **VCC_3V3**. The TPS65053 primary on-board voltage regulator operates with VCC_3V3 and generates all on-board supply voltages except 3.3V.

The phyBASE Carrier Board generates VCC_3V3 from VIN with a 3.3V voltage regulator on the Carrier Board. VIN is sourced from either the wall socket input, or a battery. The Carrier Board also controls charging the battery when the wall socket is used. You should refer to this example circuitry when designing your own Carrier Board.

See *Table 1* from *section 2* above for applicable VCC_3V3 power pins on the phyCARD-connector.

Caution:
Connect all VCC_3V3 input pins to your power supply.

As a general design rule we recommend connecting all GND pins which are neighboring signals being used in the application circuitry.

In general you should not need to adjust the Power up Mode settings. The configuration has been optimized for the phyCARD-S together with the phyBASE Carrier Board.

5 System Configuration

Although most features of the Freescale phyCARD-S microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

5.1 System Startup Configuration

During the reset cycle the i.MX27 processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitries (pull-up or pull-down resistors) are located on the phyCARD module. They are already set, so no further settings are necessary.

5.1.1 Boot Mode Select

The i.MX27 controller has different boot modes, which can be selected. The system boot mode of the processor is determined by the configuration of the four external input pins, BOOT[3:0].

Table 3: Boot Modes of i.MX27 module

Boot Mode Selection	Boot Mode/Device
0000	Bootstrap from UART/USB
0001	Reserved
0010	8-bit NAND Flash (2 Kbyte per page)
0011	16-bit Nand Flash (2 Kbyte per page)
0100	16-bit Nand Flash (512 bytes per page)
0101	16-bit CS0 (NOR-Flash)
0110	32-bit CS0
0111	8 bit Nand Flash (512 bytes per page)
1xxx	Reserved

The phyCARD-S module comes with a standard boot configuration of **'0111'**, so the system will boot from the 8-bit NAND-Flash at CS0.

6 System Memory

The phyCARD-S provides three types of on-board memory:

- LP-DDR-SDRAM: 32MByte (up to 256MByte)
- NAND Flash: 64MByte (up to 1GByte)
- I²C-EEPROM: 4KB (up to 32KByte)

It should be noted that the LP-DDR-SDRAM has a dedicated memory bus to the i.MX27 microcontroller. The LP-DDR-SDRAM bus is therefore not made available at the phyCARD-connector X2.

6.1 Memory Model

The i.MX27 memory map is summarized in Table 4 below. For a detailed view of the memory map please consult the *Freescale i.MX27 User's Manual*.

Table 4: i.MX27 memory map

ADDRESS	CHIP-SELECT	FUNCTION
0x8000 00000 – 0x8FFF FFFF	/CSD0 (/CS2)	LP-DDR-SDRAM Bank 0 (U24, U25)
0xA800 00000 – 0xAFFF FFFF	/CS1	Ethernet Controller (U38)

6.2 LP-DDR-SDRAM (U24-U25)

The phyCARD-S can use one, or both of the LP-DDR-SDRAM banks on the i.MX27 depending on the SDRAM population density options.

Each RAM bank is comprised of two 16-bit wide DDR-SDRAM chips, configured for 32-bit access, and operating at 133MHz. In lower density configurations, U24 and U25 populate the module and are accessed via SDRAM memory bank 0 using chip select signal /CSD0 starting at 0x8000 0000. In higher density configurations, U24 and U25 are also populated and are accessed via SDRAM memory bank 1 using chip select signal /CSD1 starting at 0x9000 0000.

Typically the LP-DDR-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX27 controller. Refer to the i.MX27 User Manual for accessing and configuring these registers.

6.3 NAND Flash Memory (U16)

Use of Flash as non-volatile memory on the phyCARD-S provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCARD-S:

Table 5: Compatible NAND Flash devices

MANUFACTURER	NAND FLASH P/N	DENSITY (MBYTE)
ST Microelectronics	NAND512W3A2CN6	64

Additionally, any parts that are footprint (VFBGA) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCARD-S.

These Flash devices are programmable with 1.8 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

6.4 I²C EEPROM (U28)

The phyCARD-S is populated with a ST 24W32C[1] non-volatile 4KByte EEPROM (U28) with an I²C interface to store configuration data or other general purpose data. This device is accessed through I²C port 2 on the i.MX27.
Three solder jumpers are provided to set the lower address bits: J3, J4 and J5. *Refer to section 6.4.1 for details on setting these jumpers.*

Write protection to the device is accomplished via jumper J2. By default this jumper is closed, allowing write access to the EEPROM. Removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device. *Refer to section 6.4.2 for further details on setting this jumper.*

1: See the manufacturer's data sheet for interfacing and operation.

6.4.1 Setting the EEPROM Lower Address Bits (J3, J4, J5)

The 32KB I²C EEPROM populating U28 on the phyCARD-S module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see ST 24W32C data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J3, J4 and J5. J4 sets address bit A0, J3 address bit A1, and J5 address bit A2.

Table 6 below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

Table 6: U28 EEPROM I²C address via J3, J4, and J5[1]

U28 I²C DEVICE ADDRESS	J5	J3	J4
1010 010	**2 + 3**	**2 + 3**	**2 + 3**
1010 011	2 + 3	2 + 3	1 + 2
1010 000	2 + 3	1 + 2	2 + 3
1010 001	2 + 3	1 + 2	1 + 2
1010 110	1 + 2	2 + 3	2 + 3
1010 111	1 + 2	2 + 3	1 + 2
1010 100	1 + 2	1 + 2	2 + 3
1010 101	1 + 2	1 + 2	1 + 2

[1] Defaults are in **bold blue** text

6.4.2 EEPROM Write Protection Control (J2)

Jumper J2 controls write access to the EEPROM (U28) device. Closing this jumper allows write access to the device, while opening this jumper enables write protection.

The following configurations are possible:

Table 7: EEPROM write protection states via J2[1]

EEPROM WRITE PROTECTION STATE	J8
Write access allowed	**open**
Write protected	closed

[1] Defaults are in **bold blue** text

7 Serial Interface

7.1 UART1 (U26)

The phyCARD-S does not convert the UART1 provided by the i.MX27 MCU to RS-232 levels. The TTL level signals are made available at the phyCARD-connector X2 (*see Table 1*). External RS-232 transceivers must be supplied by the user if additional UART's require RS-232 levels.

- RXD1/TXD1/RTS1/CTS1 (UART1)

8 USB-OTG Transceiver (U34)

The phyCARD-S comes populated with a NXP ISP1504 USB On-The-Go High-Speed transceiver (U34) supporting high speed, full speed, and low speed data rates. The ISP1504 functions as the transceiver between the i.MX27 Host Controller, Device Controller, and On-The-Go Controller. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCARD-S USB OTG functionality. The applicable interface signals (D+/D-/VBUS/ID) can be found in the phyCARD-connector pin-out *Table 1.*

9 USB-HOST Transceiver (U35)

The phyCARD-S comes populated with a NXP ISP1504 USB HOST High-Speed transceiver (U35) supporting high speed, full speed, and low speed data rates. The ISP1504 functions as the transceiver between the i.MX27 Host Controller, Device Controller, and HOST Controller. An external USB Standard-A (for USB host connector is all that is needed to interface the phyCARD-S USB OTG functionality. The applicable interface signals (D+/D-/VBUS/ID) can be found in the phyCARD-connector pin-out *Table 1.*

10 Ethernet Controller / Ethernet-Phy (U38)

Connection of the phyCARD-S to the world wide web (WWW) or a local area network (LAN) is possible with the internal 10/100 Mbps Fast Ethernet controller. With this Ethernet controller an external transceiver interface and transceiver function are required to complete the interface to the media. Therefor the i.MX27 uses an Ethernet-Phy (U38).

The Ethernet-Phy provides MII/RMII/SMII interfaces to transmit and receive data. In addition the PHY also supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet-Phy also features LinkMD cable diagnostics, which allows detection of common cabling plant problems such as open and short circuits.

The physical memory area for the Fast Ethernet controller is defined in Table 8.

Table 8: Fast Ethernet controller memory map

ADDRESS	FUNCTION
0x1002_B + 0x000-1FF	Control/Status Registers
0x1002_B + 0x200-3FF	MIB Block Counters

Connection to an external Ethernet transformer should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

Caution!
Please note the datasheet of the Ethernet-Phy when creating the Ethernet transformer circuitry.

11 JTAG Interface (X1)

The phyCARD-S is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends out to a 2.0 mm pitch pin header at X1 on the edge of the module PCB. *Figure 8* and *Figure 9* show the position of the debug interface (JTAG connector X1) on the phyCARD-S module.

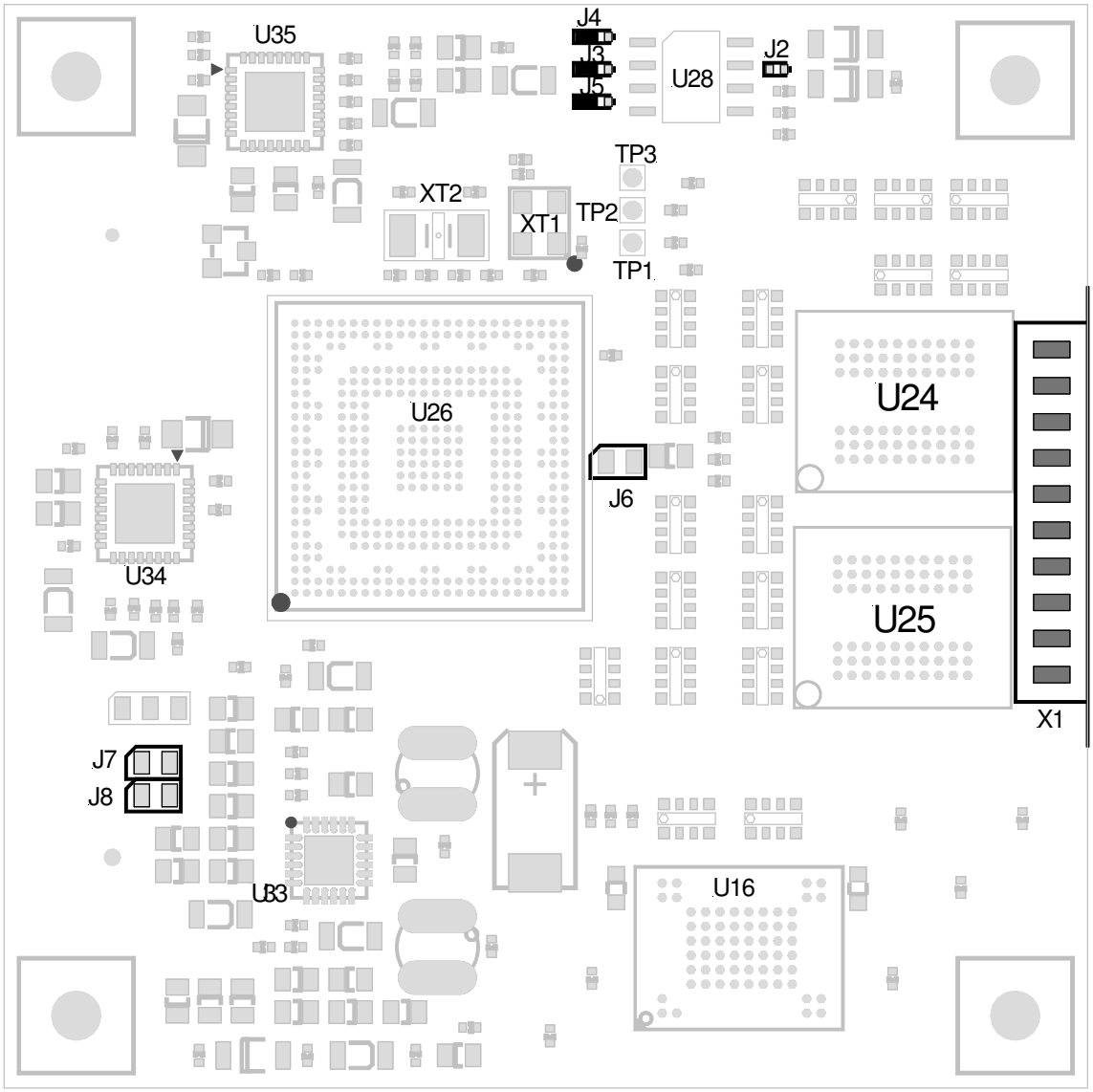


Figure 8: JTAG interface at X1 (top view)

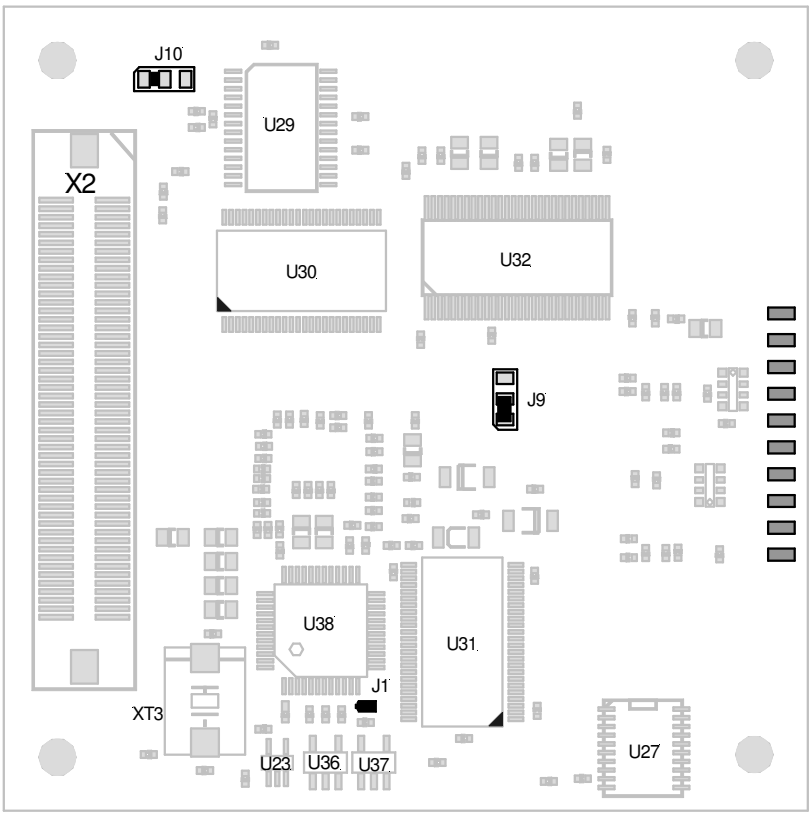


Figure 9: JTAG interface at X1 (bottom view)

Pin 1 of the JTAG connector X1 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Note:
The JTAG connector X1 only populates phyCARD-S modules with order code PCA-100-D. JTAG connector X1 is not populated on phyCARD modules with order code PCA-100. We recommend integration of a standard (2 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See*
Table 9 *for details on the JTAG signal pin assignment.*

Table 9: JTAG connector X1 signal assignment

SIGNAL	PIN ROW*		SIGNAL
	A	B	
VCCLOGIC	2	1	VTref (VCCLOGIC via 100 Ohm)
GND	4	3	x_CPU_/TRST
GND	6	5	x_CPU_TDI
GND	8	7	x_CPU_TMS
GND	10	9	x_CPU_TCK
GND	12	11	x_CPU_RTCK
GND	14	13	x_CPU_TDO
GND	16	15	x_/RESET_MCU
GND	18	17	x_CPU_/DE
GND	20	19	J_DBGACK (10k Ohm pulldown)

*Note: Row A is on the controller side of the module and row B is connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCARD-S to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X1 to standard Emulator connectors.

12 Technical Specifications

The physical dimensions of the phyCARD-S are represented in Figure 10. The module's profile is approximately ***8.5 mm*** thick, with a maximum component height of ***4.0 mm*** on the bottom (connector) side of the PCB and approximately ***3.1 mm*** on the top (microcontroller) side. The board itself is approximately ***1.4 mm*** thick.

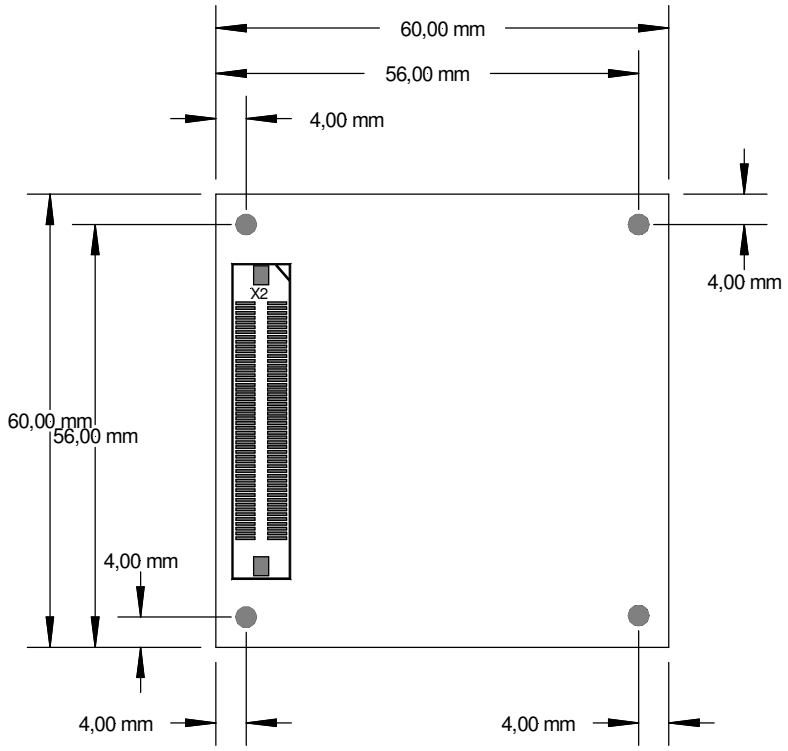


Figure 10: Physical dimensions

Additional specifications (***all TBD***):

• *Dimensions:*	*60 mm x 60 mm*
• *Weight:*	*approximately 16 g with all optional components mounted on the circuit board*
• *Storage temperature:*	*-40 °C to +125 °C*
• *Operating temperature:*	*0 °C to +70 °C (commercial)* *-40 °C to +85 °C (industrial)*
• *Humidity:*	*95 % r.F. not condensed*
• *Operating voltage:*	*VCC 3.3V*
• *Power consumption:* *VCC 3.3 V/100mA typical*	*Conditions:* ***VCC = 3.3 V, VBAT = 3 V,*** *32MB LP-DDR-RAM, 64MB NAND-Flash, Ethernet, 400 MHz CPU frequency at 20 °C*

These specifications describe the standard configuration of the phyCARD-S as of the printing of this manual.

13 Hints for Handling the phyCARD-S

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

14 The phyCARD-S on the phyBase

PHYTEC phyBASE Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. phyBASE Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

14.1 Concept of the phyBASE Board

The phyBASE Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCARD Single Board Computer module. The Carrier Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation. The Carrier Board is compatible with all phyCARD

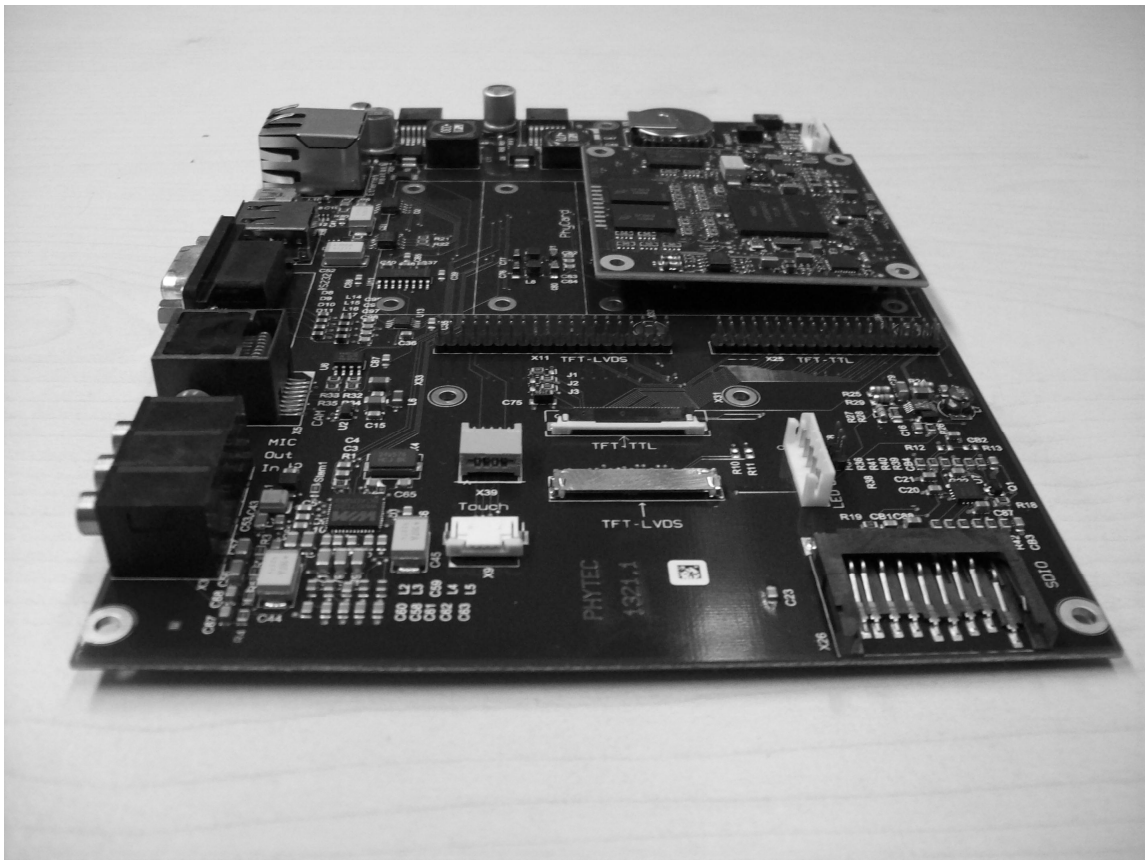


Figure 11: phyCARD-S Carrier Board connection

This modular development platform concept depicted in **Fehler! Verweisquelle konnte nicht gefunden werden.** below includes the following components:

- The **phyCARD-S Module** – contains the i.MX27 processor and all applicable SBC circuitry such as DDR SDRAM, Flash, PHYs, and transceivers to name a few.

- The **phyBASE Carrier Board** – which offers all essential components and connectors for start-up and connection to processor peripherals.

The following sections contain specific information relevant to the operation of the phyCARD-S mounted on the phyBASE Carrier Board.

14.2 Connectors

Table 10 lists all available connectors on the phyBASE. Figure 12 highlights the location of each connector for easy identification.

Table 10: Carrier Board connectors

REFERENCE DESIGNATOR	DESCRIPTION
X1	Stereo Microphone input connector
X2	Stereo Speaker output connector
X3	Stereo Line In input connector
X5	Camera Interface, RJ45
X6	LVDS-LCD DF19G-20P
X7	TTL-LCD FCC40
X8	LED-Backlight connector FPC4
X9	Touch screen CIF connector
X10	Ethernet connector, RJ45 with speed and link led
X11	LVDS and touch screen pin header connector, 2*20 pins, 2 mm spacing
X24	SPI connector, 2*8 pins, 2 mm spacing
X25	TTL-LCD pin header connector, 2*20 pins, 2 mm spacing
X26	Security Digital/MultiMedia Card socket
X27	phyCARD-connector for mounting the phyCARD-S up to phyCARD-L
X28	Socket for +12-24 volt power supply connectivity
X29	USB On-The-Go connector
X30	USB Host connector
P1	First Serial Interface, DB-9F

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user‘s responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

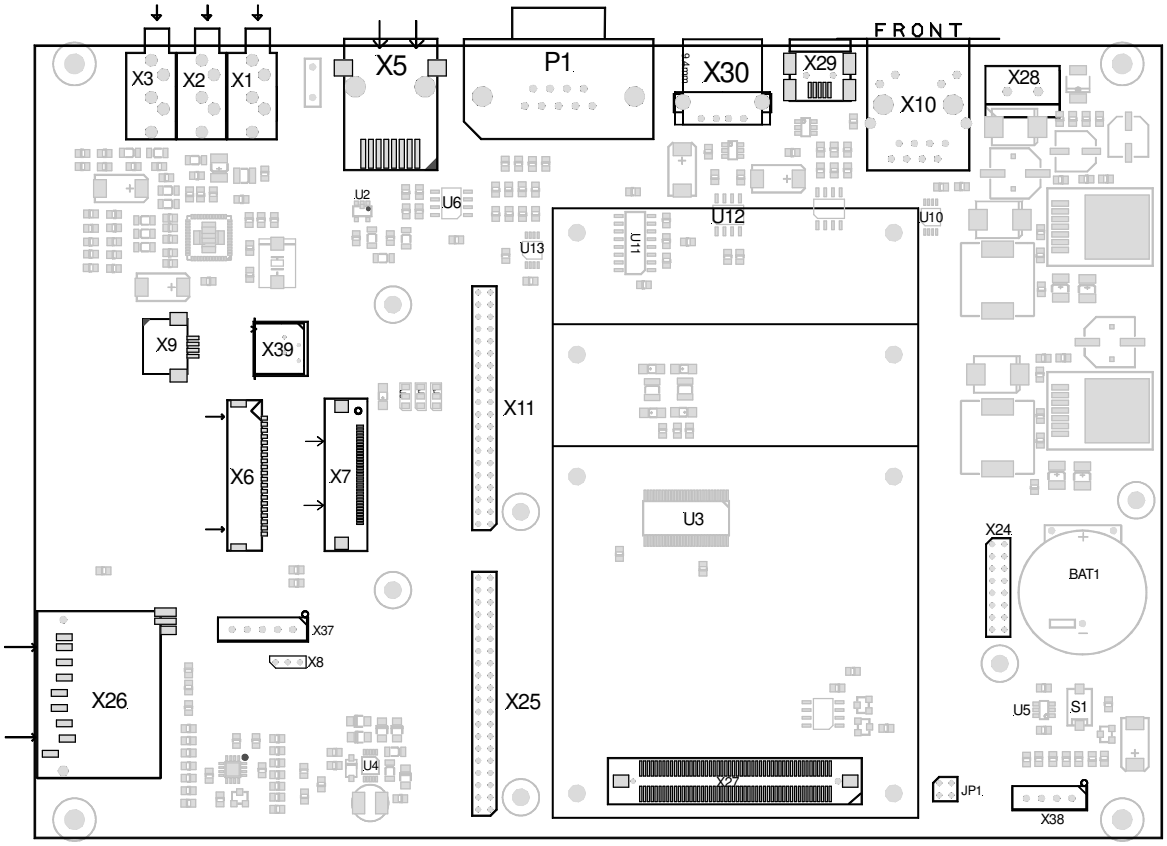


Figure 12: Carrier Board connector locations

14.3 Jumpers

Carrier Board jumpers allow a variety of signal configurations and connectivity options between the phyCARD-S module and Carrier Board peripheral connectors. Before making connection to peripheral connectors it is a good idea to consult the applicable section in this manual for setting the associated jumpers.

See Table 11 for default settings and descriptions of all Carrier Board jumpers.

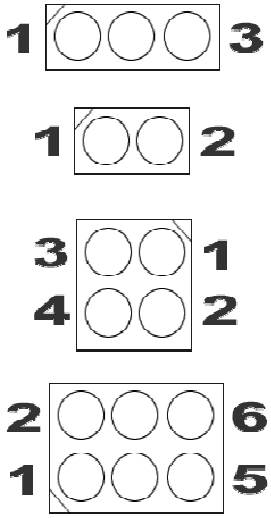


Figure 13: Typical jumper numbering scheme

Figure 13 illustrates the numbering scheme for various jumper blocks. Note that in each case pin 1 is always marked with a clipped corner on the PCB silk screen. Figure 14 highlights the locations of all user configurable jumpers on the phyBASE Carrier Board.

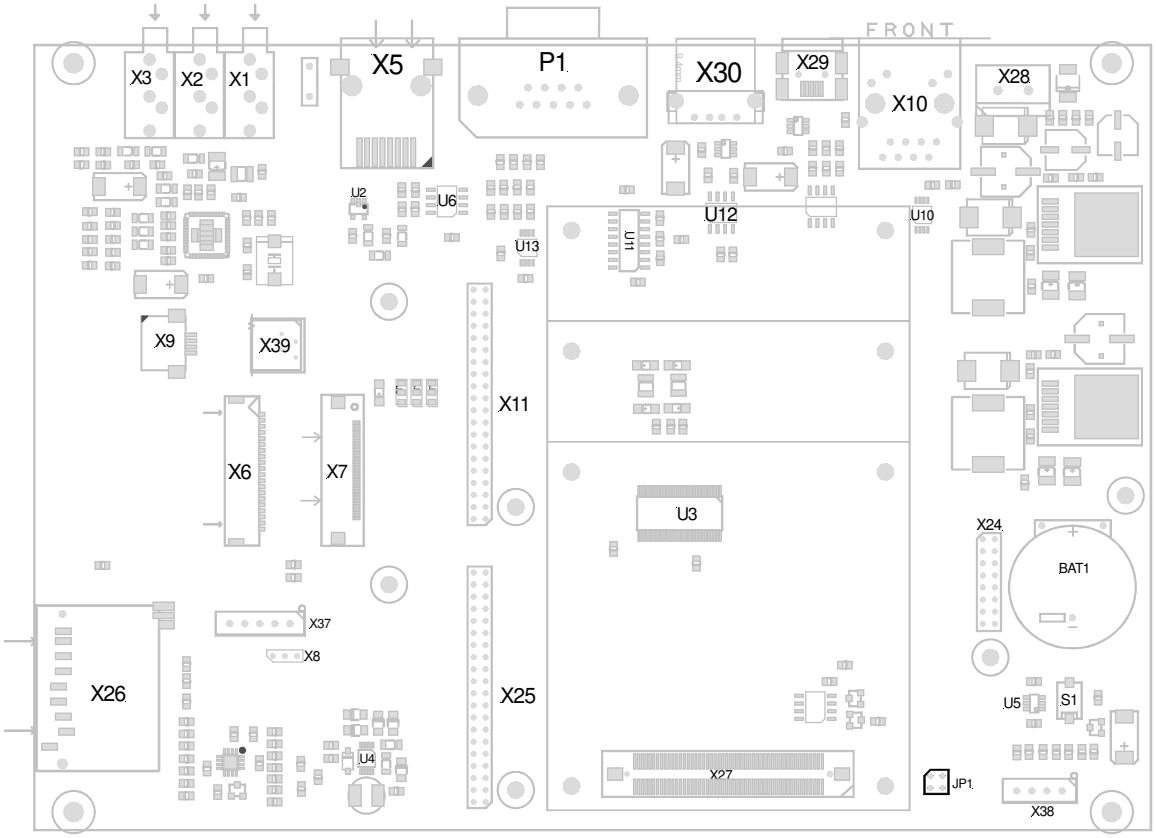


Figure 14: Carrier Board jumper locations

Table 11: Carrier Board jumper descriptions[1]

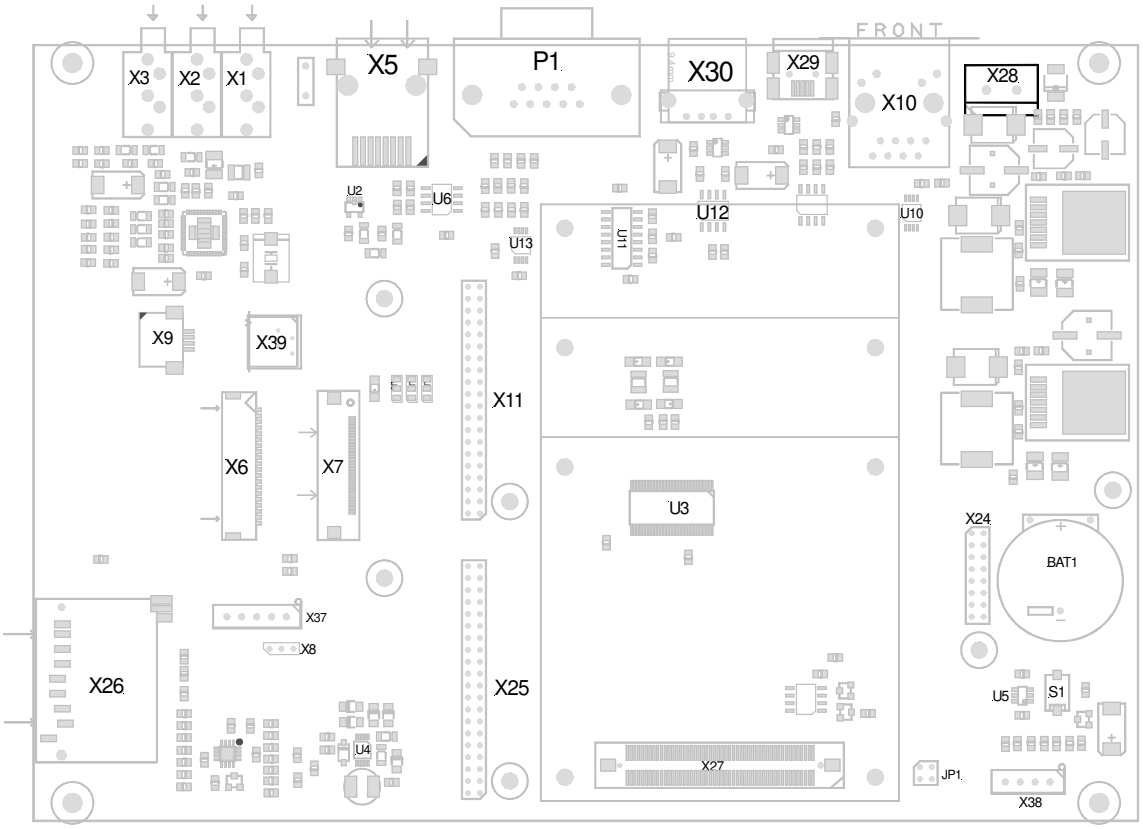
JUMPER	SETTING	DESCRIPTION	SEE SECTION
JP1	**Open**	**FLASH Boot device are enabled**	14.4.2
	1+2	Ethernet Boot device are enabled	
	3+4	RS-232/USB Boot device are enabled	
	1+2,3+4	SD/MMC Boot device are enabled	

[1] Default settings are in **bold blue** text

14.4 Functional Components on the phyBASE Board

This section describes the functional components of the phyBASE Carrier Board supporting the phyCARD-S. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

14.4.1 Power Supply (X28)



Caution:
Do not use a laboratory adapter to supply power to the Carrier Board! Power spikes during power-on could destroy the phyCARD-module mounted on the Carrier Board! Do not change modules or jumper settings while the Carrier Board is supplied with power!

Figure 15: Power adapter

14.4.2 RS-232 Interfaces (P1)

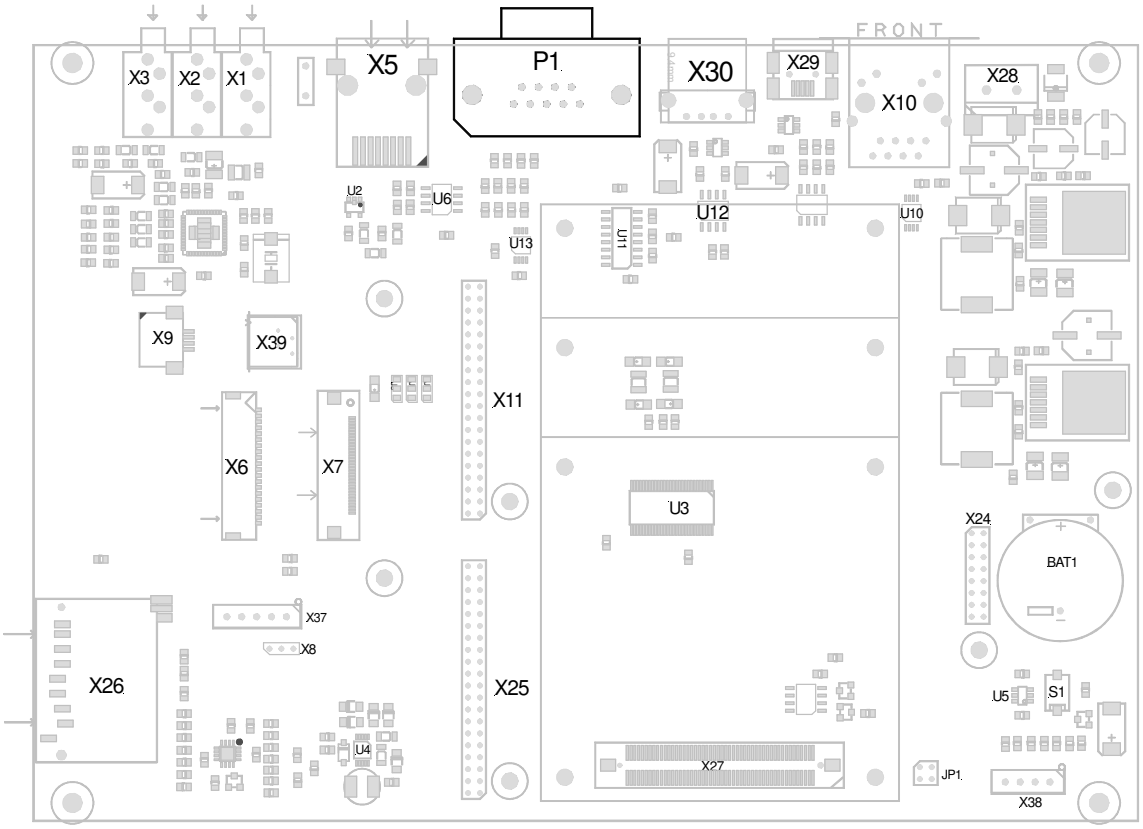


Figure 16: UART1 connection interface at connector P1

Connector P1 provides a connection interface to the phyCARD UART1 serial interfaces. P1 is a DB9 sub-connectors called P1.

14.4.2.1 UART1 (P1)

UART1 provides only two handshake signals: RTS and CTS. Figure 17 below shows the signal mapping of the RS-232 level signals to connector P1A.

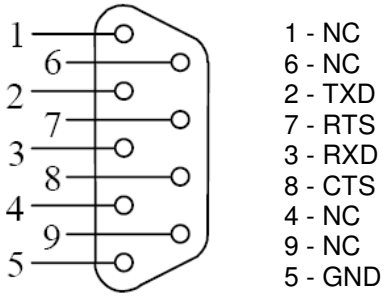


Figure 17: UART1 connector P1 signal description

14.4.3 Push Buttons

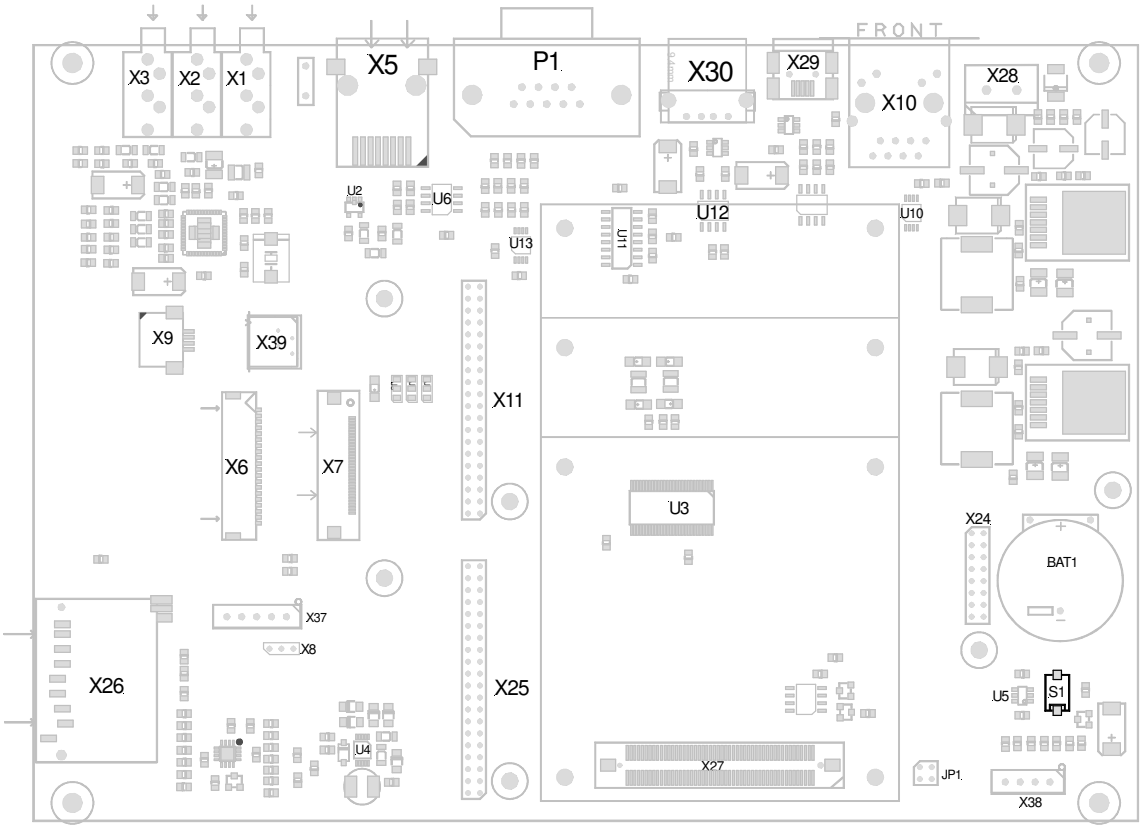


Figure 18 - Button locations

The phyBASE provides a variety of buttons for input, feedback, and status purposes. A detailed description of each button and LED is presented below.

S1 Issues a **system reset** signal. Momentarily pressing this button will toggle the nRESET_IN pin of the phyCARD microcontroller LOW, causing the controller to reset.

14.4.4 Security Digital Card/ MultiMedia Card (X26)

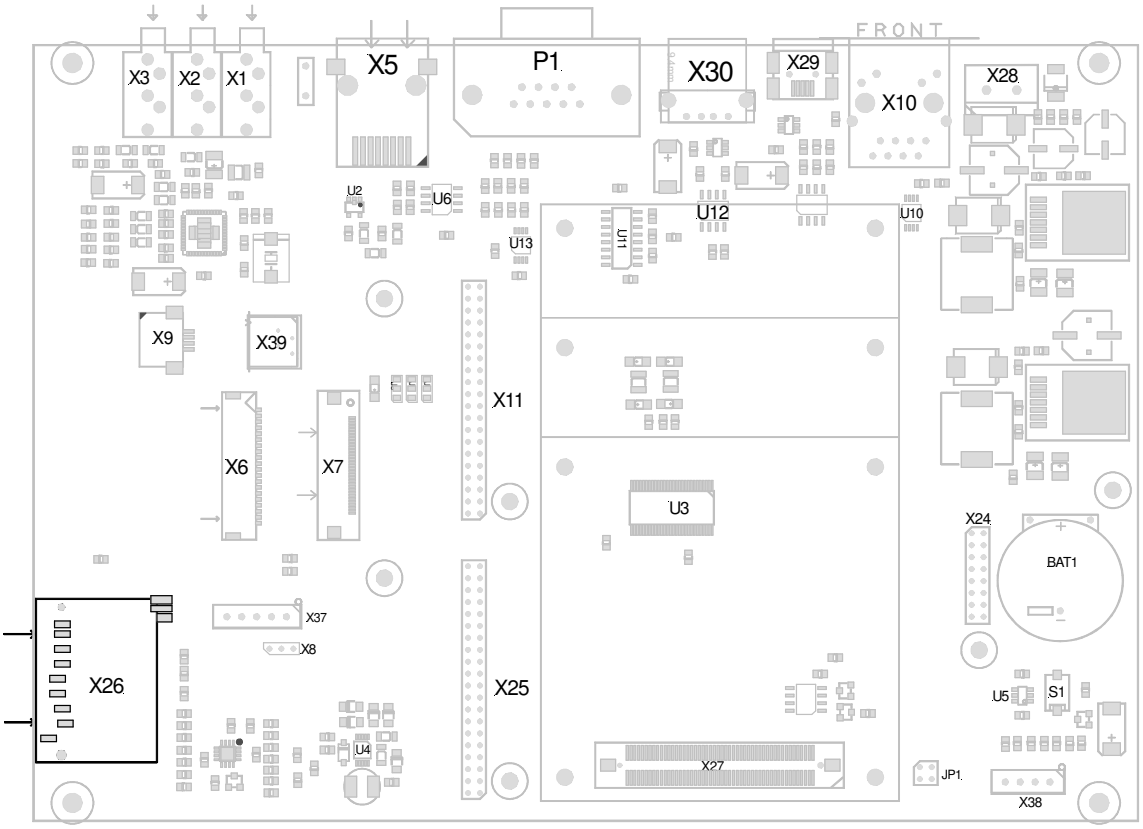


Figure 19: SD Card interface at connector X26

A Security Digital interface is available on the baseboard at X26.

14.4.5 Ethernet Interface (X10)

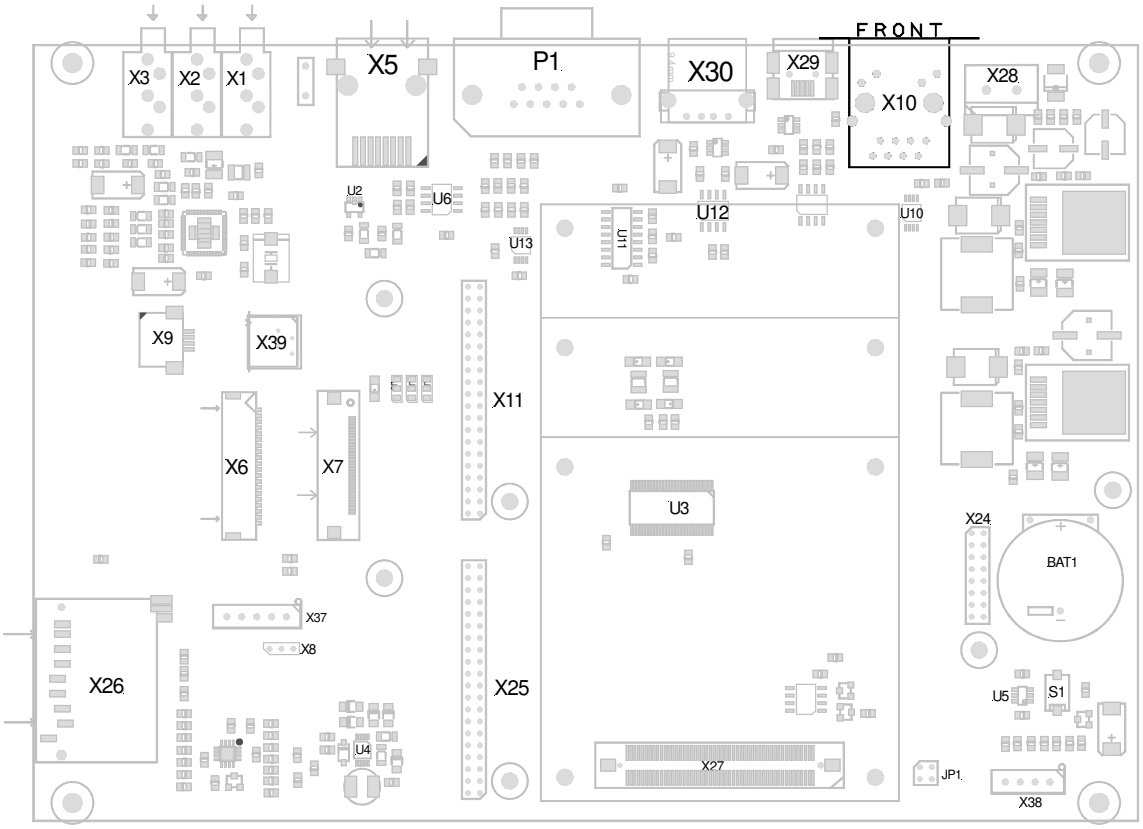


Figure 20: Ethernet interface at connector X10

The Ethernet interface is supplemented on the baseboard by the Ethernet transformer and the RJ45 connector.

The Ethernet interface is accessible on the RJ45 socket at X10. The yellow LED extends to the x_ETH_/LED1 signal (Speed indicator) and the green LED extends to x_ETH_/LED2 (Link/Activity).

14.4.6 USB Host (X30)

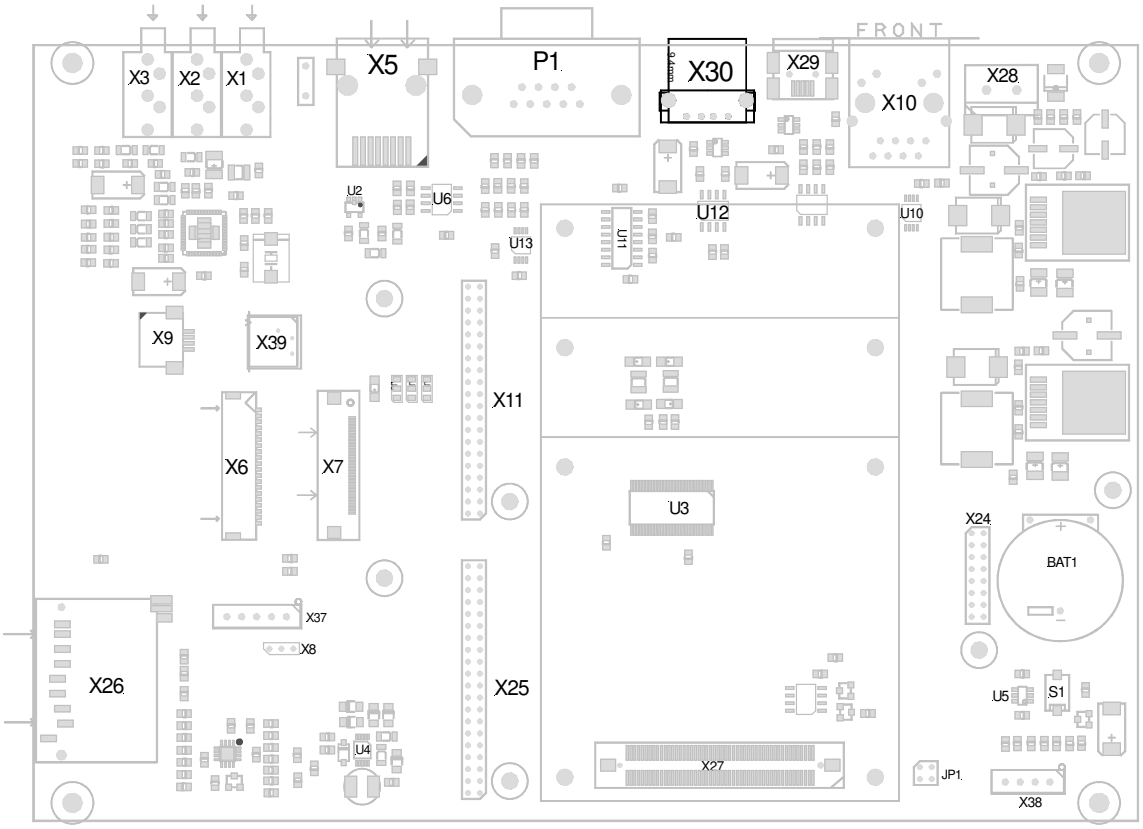


Figure 21: USB host interface at connector X30

The controller supports control of input USB devices such keyboard, mouse or USB key. The connector type of X30 is USB A.

14.4.7 USB OTG (X29)

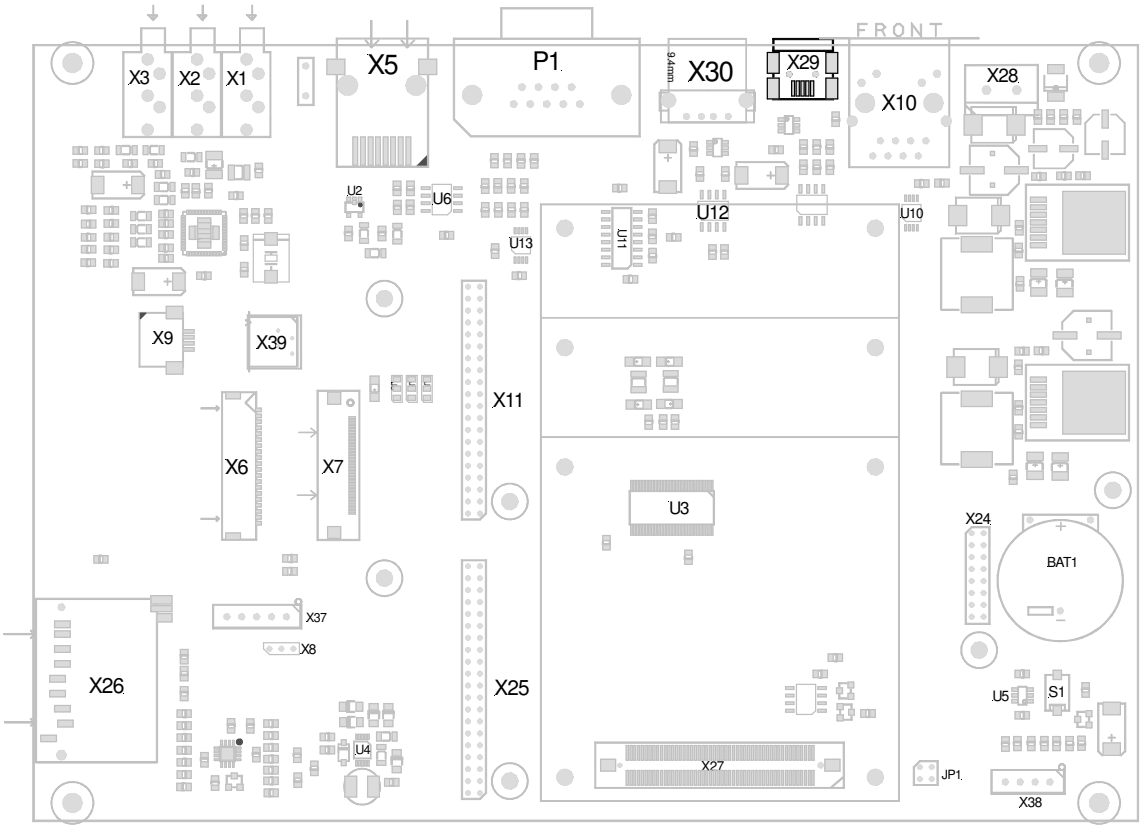


Figure 22: USB OTG interface at connector X29

The controller supports the On-The-Go feature. The Universal Serial Bus On-The-Go is a device capable to initiate the session, control the connection and exchange Host/Peripheral roles between each other. The connector type of X29 is USB Mini AB.

14.4.8 Universal LCD Pin Header (X7,X25)

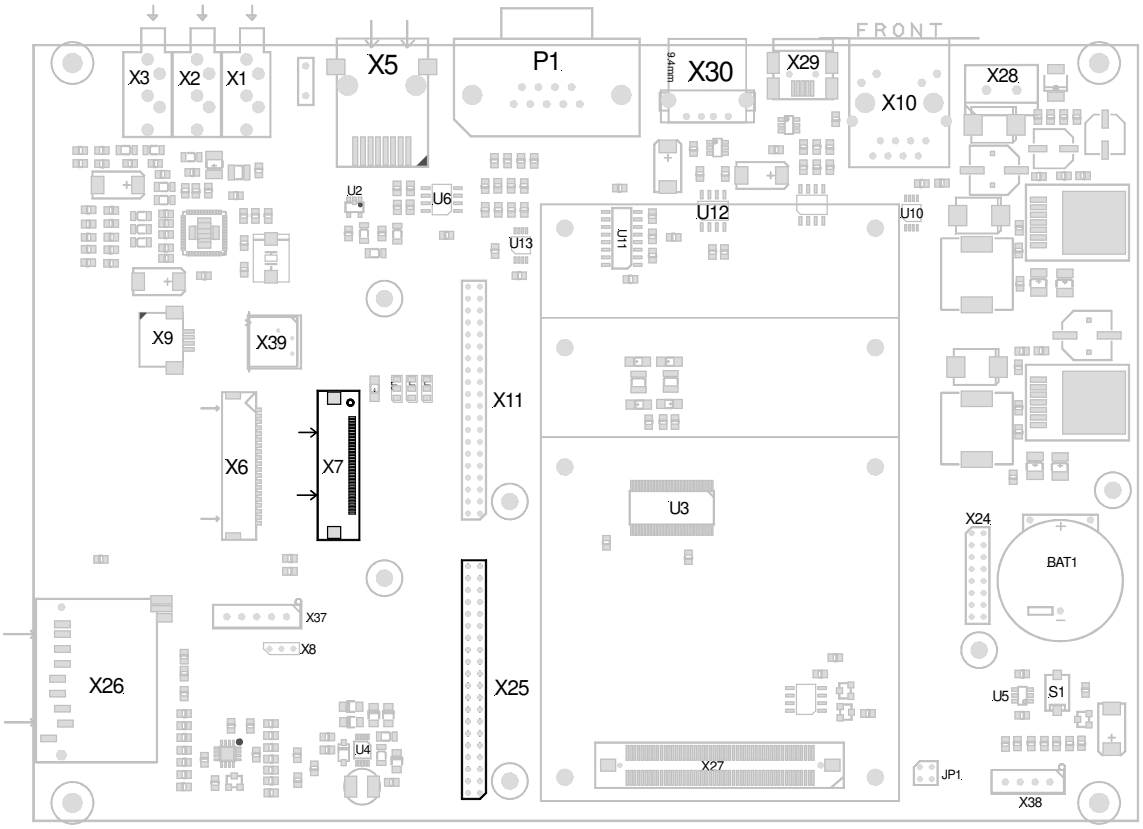


Figure 23: Universal LCD interface at connector X7,X25

Pin header connector X7, X25 provides a connection to the phyBASE LCD interface.

Table 12 provides a detailed list of the signals found at X7,X25. You should consult the LCD interface section of the phyBASE schematics when connecting to a custom LCD interface.

Table 12: Universal LCD pin header signal description

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	VCC3V3	LCD power
2	VCC3V3	LCD power
3	VCC5V	5V power supply

4	VCC5V	5V power supply
5	GND	Ground
6	LCD_PCLK	
7	GND	Ground
8	LCD_R0	Red data 0
9	LCD_R1	Red data 1
10	LCD_R2	Red data 2
11	LCD_R3	Red data 3
12	LCD_R4	Red data 4
13	LCD_R5	Red data 5
14	LCD_R6	Red data 6
15	LCD_R7	Red data 7
16	GND	Ground
17	LCD_G0	Green data 0
18	LCD_G1	Green data 1
19	LCD_G2	Green data 2
20	LCD_G3	Green data 3
21	LCD_G4	Green data 4
22	LCD_G5	Green data 5
23	LCD_G6	Green data 6
24	LCD_G7	Green data 7
25	GND	Ground
26	LCD_B0	Blue data 0
27	LCD_B1	Blue data 1
28	LCD_B2	Blue data 2
29	LCD_B3	Blue data 3
30	LCD_B4	Blue data 4
31	LCD_B5	Blue data 5
32	LCD_B6	Blue data 6
33	LCD_B7	Blue data 7
34	GND	Ground
35	LCD_RESET	
36	LCD_LCLK	
37	LCD_FCLK	
38	LCD_ENAB	LCD enable
39	GPIO2_IRQ	
40	GND	Ground

14.4.9 Universal LVDS Pin Header (X6,X11)

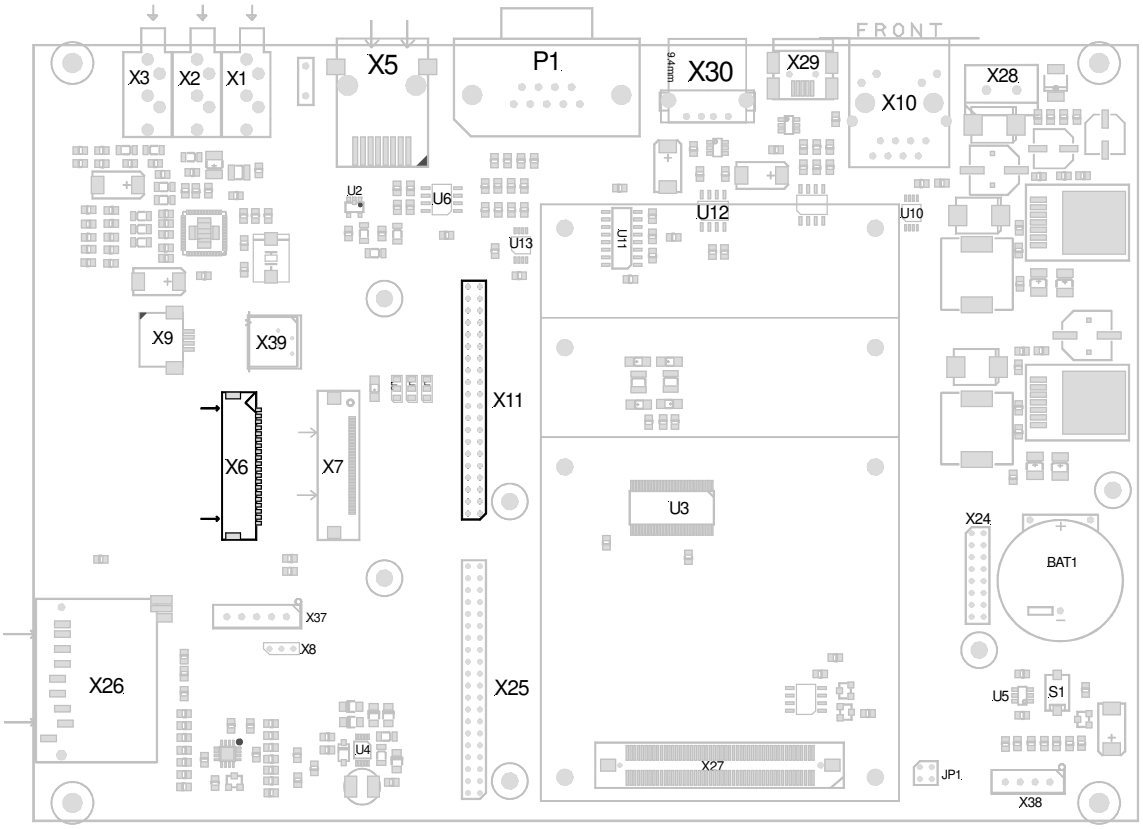


Figure 24: Universal LCD interface at connector X6,X11

Pin header connector X11 provides a connection to the phyBASE LCD interface.

Table 12 provides a detailed list of the signals found at X11. You should consult the LVDS interface section of the phyBASE schematics when connecting to a custom LVDS interface.

Table 13: Universal LCD pin header signal description

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	TXOUT0+	LVDS_OUT0+

4	TXOUT1+	LVDS_OUT1+
5	TXOUT0-	LVDS_OUT0-
6	TXOUT1-	LVDS_OUT1-
7	GND	Ground
8	GND	Ground
9	TXOUT2+	LVDS_OUT2+
10	TXOUT3+	LVDS_OUT3+
11	TXOUT2-	LVDS_OUT2-
12	TXOUT3-	LVDS_OUT3-
13	GND	Ground
14	GND	Ground
15		Not connected
16	TXCLKOUT+	LVDS_CLK+
17		Not connected
18	TXCLKOUT-	LVDS_CLK-
19	GND	Ground
20	GND	Ground
21	LCD_I2C_SDA	I2C Data
22		Not connected
23	LCD_I2C_SCL	I2C Clock
24		Not connected
25	GND	Ground
26		Not connected
27		Not connected
28		Not connected
29		Not connected
30		Not connected
31	GND	Ground
32		Not connected
33	TP_Y+	Touch
34	TP_X+	Touch
35	TP_X-	Touch
36	TP_Y-	Touch
37	GND	Ground
38		Not connected
39	VCC3V3	LCD power
40	GND	Ground

14.4.10 Camera Interface (X5)

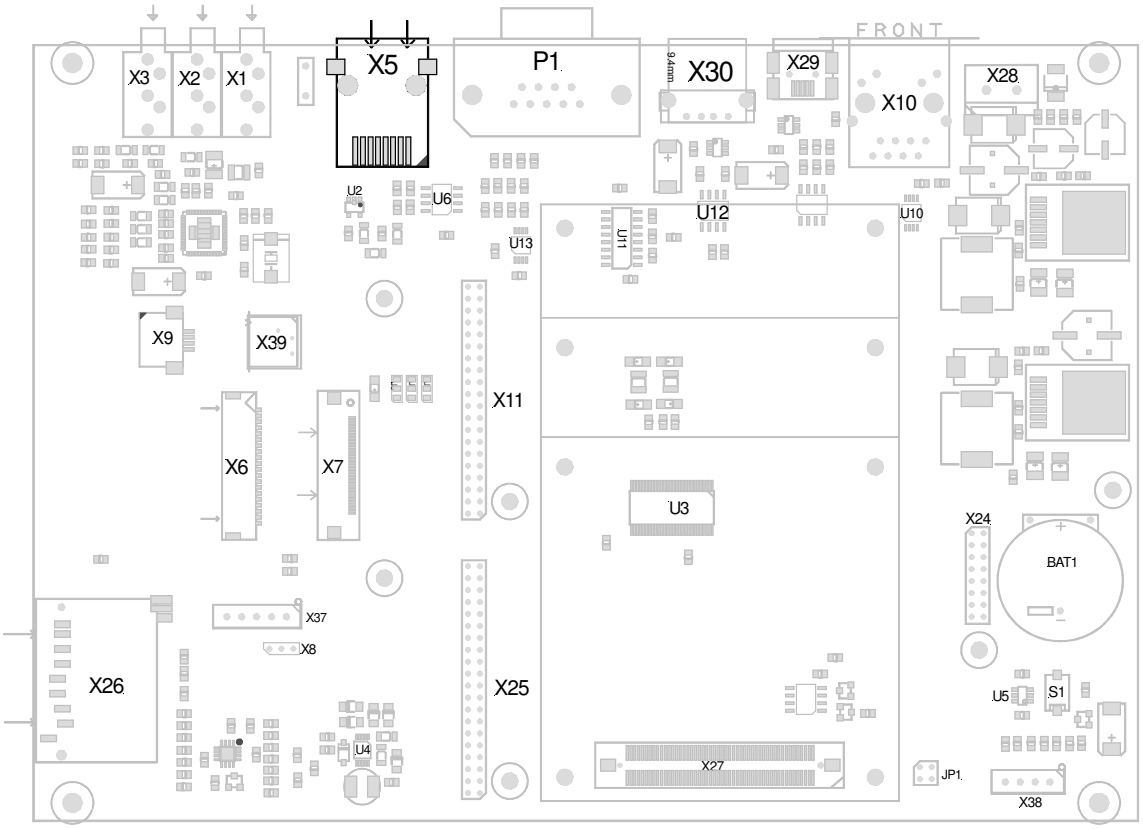


Figure 25: Camera interface at connectors X5

The pin-out of the connector X5 is shown in the table below:

Table 14: PHYTEC camera connector X5

PIN #	SIGNAL NAME	DESCRIPTION
1	RXIN+	LVDS Input+
2	RXIN-	LVDS Input-
3	RX_CLK+	LVDS Clock+
4	LCD_I2C_SDA	I2C Data
5	LCD_I2C_SCL	I2C Clock
6	RXCLK-	LVDS Clock-
7	VCC_CAM	Power supply camera
8	GND	Ground

14.4.11 Touch Interface (X9,X39)

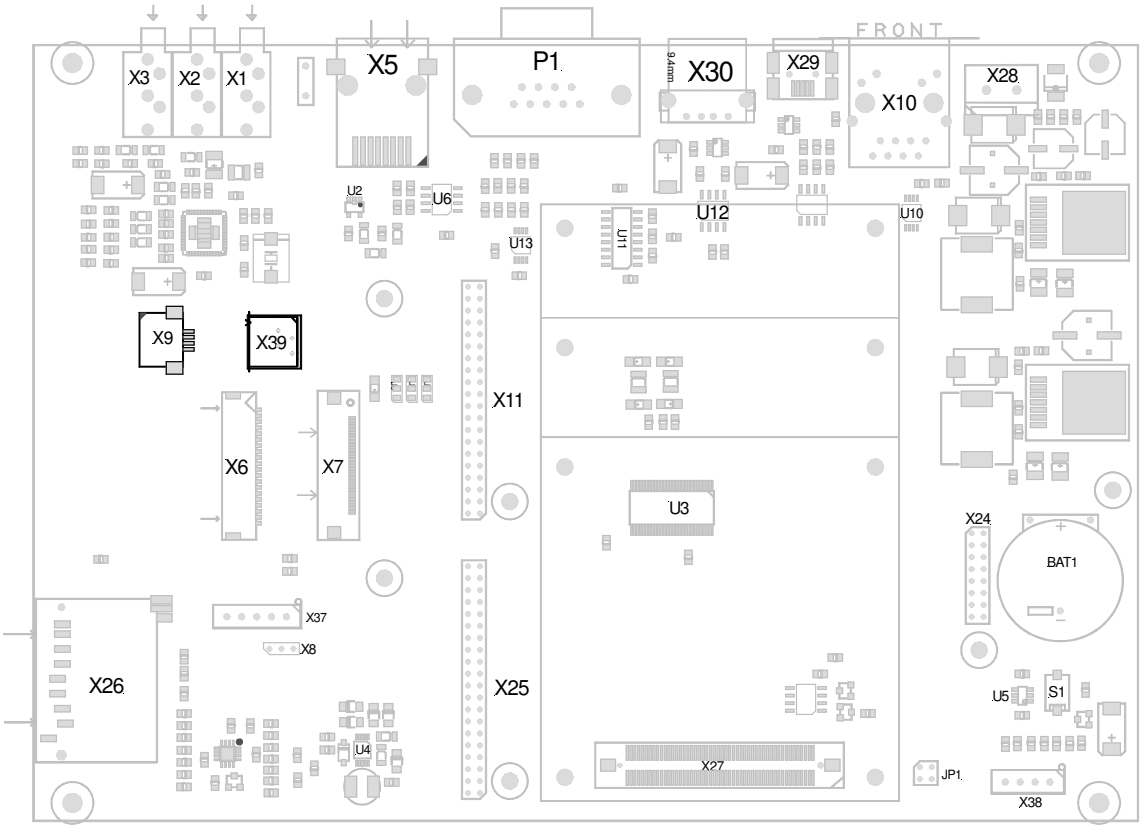


Figure 26: Touch interface at connectors X9, X39

14.4.12 Audio Interface (X1,X2,X3)

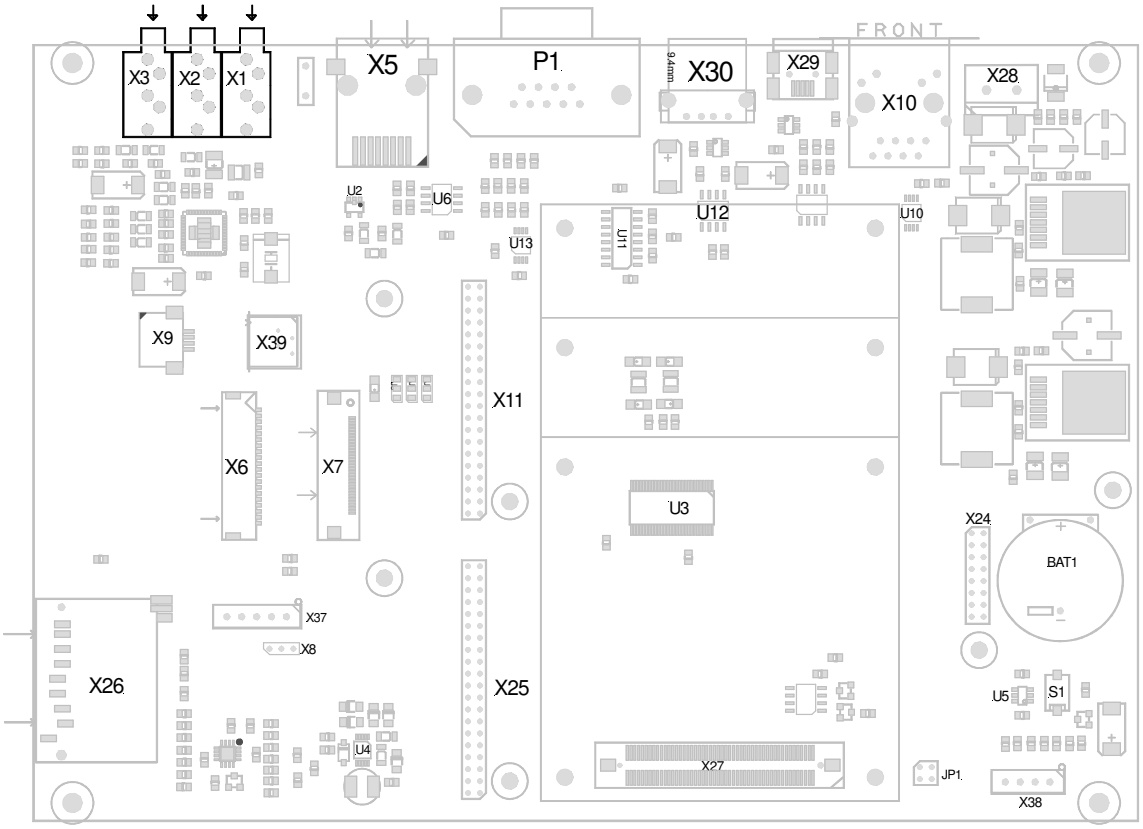


Figure 27: Audio interface at connectors X1,X2,X3

14.4.13 LED Backlight Interface (X8,X37)

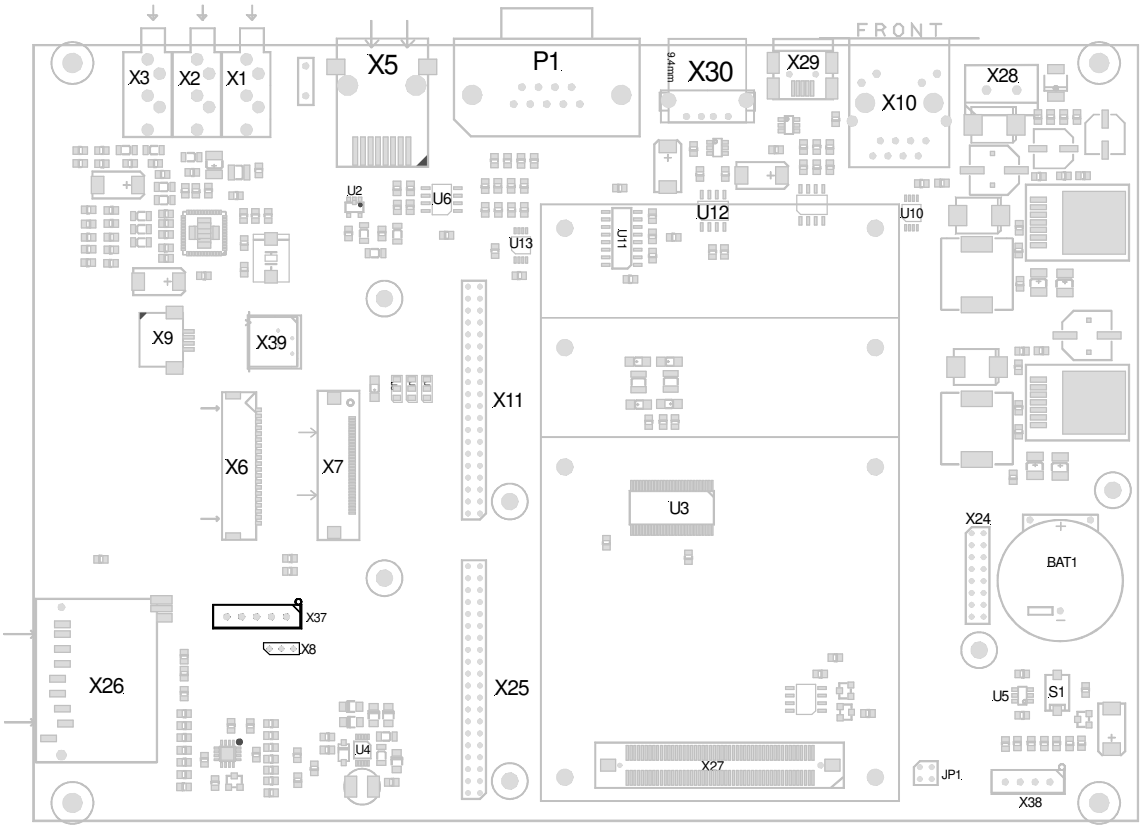


Figure 28: Led Backlight interface at connectors X8,X37

14.4.14 CCFL Connector (X38)

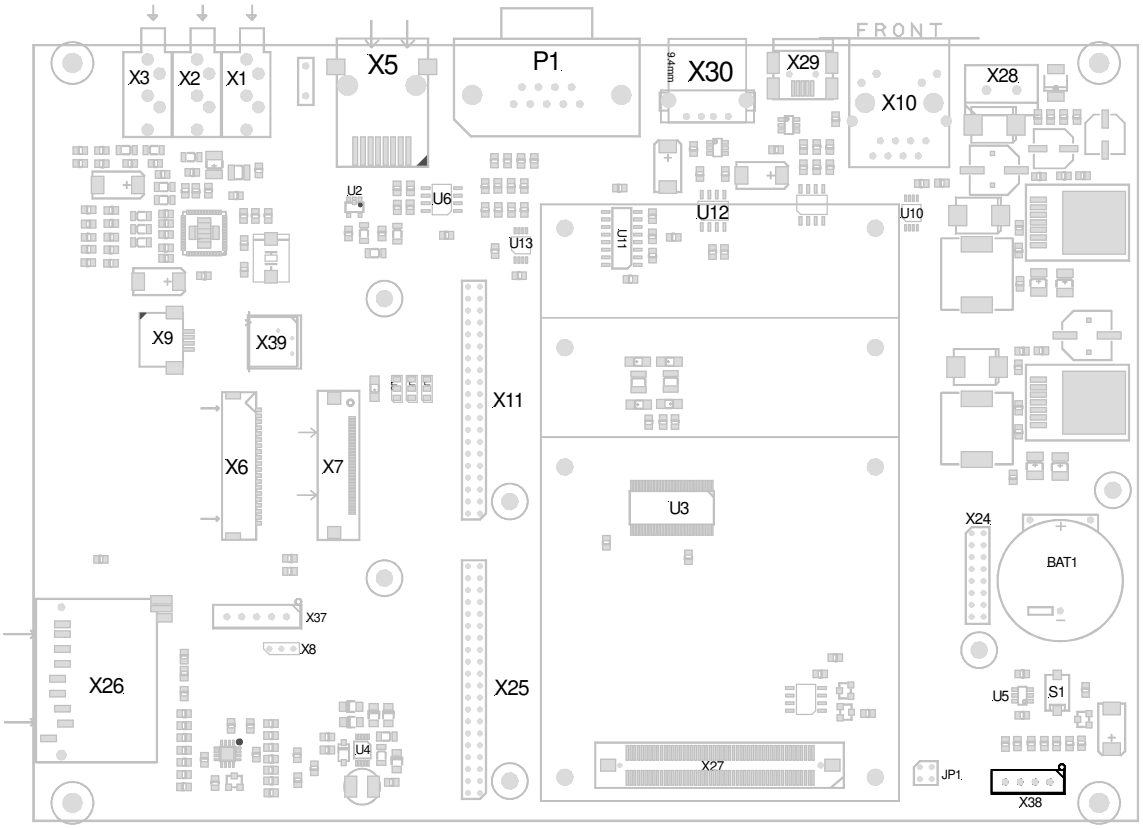


Figure 29: CCFL connector X38

14.4.15 Expansion Interface (X24)

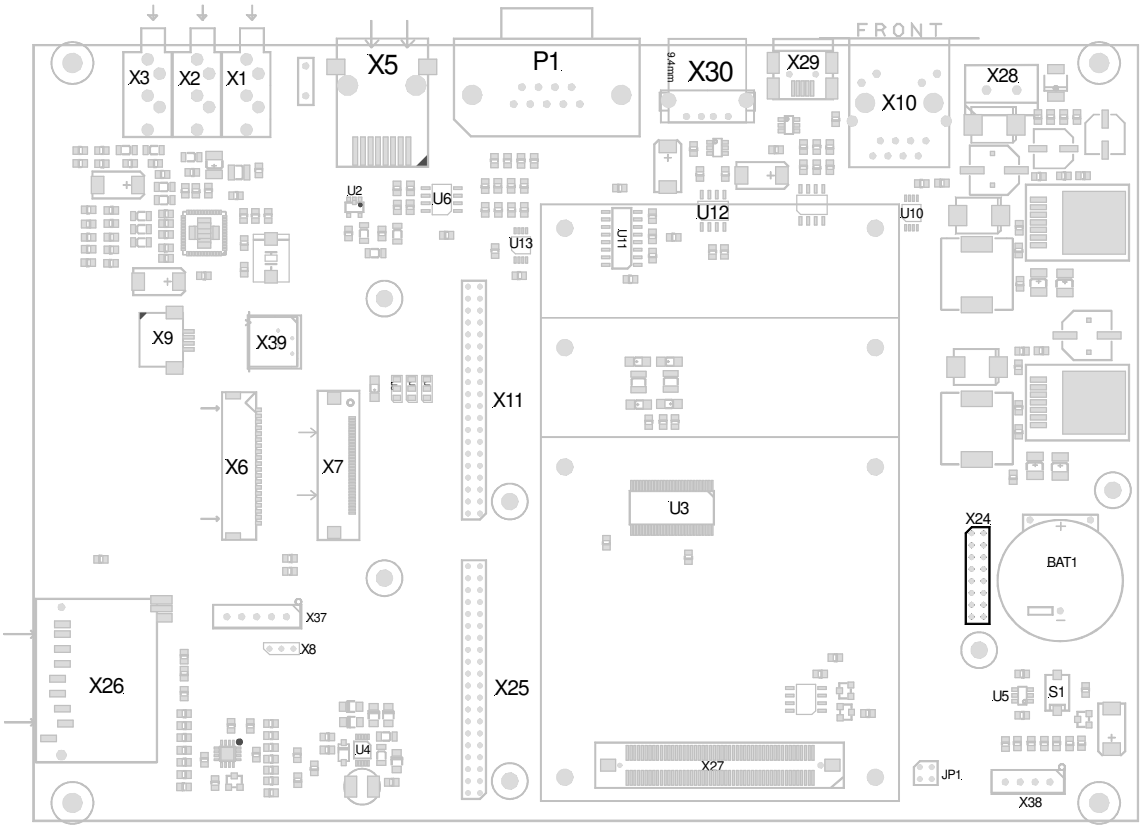


Figure 30: Expansion interface at connectors X24

14.4.16 Carrier Board Physical Dimensions

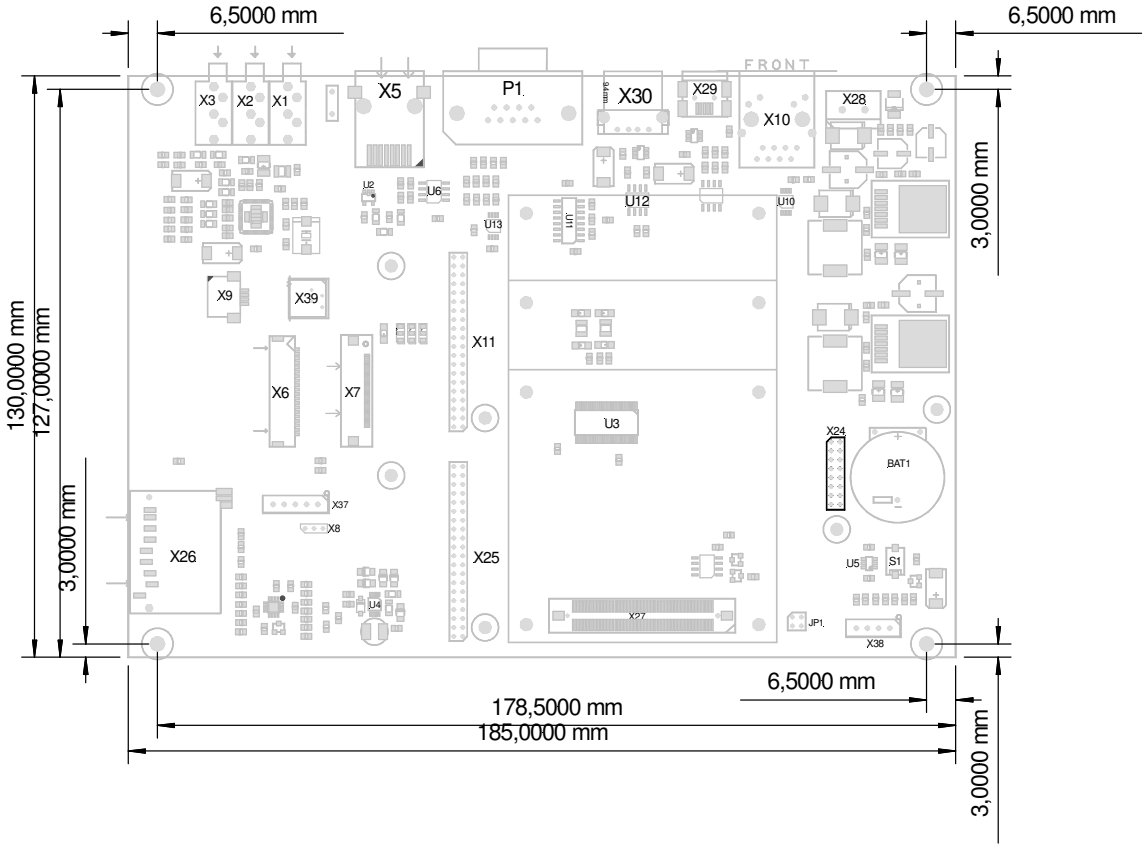


Figure 31: Carrier Board Physical Dimensions

15 Revision History

Date	Version numbers	Changes in this manual
01-07-2009	Manual L-731e_0	First draft, Preliminary documentation. Describes the phyCARD-S with phyBASE-Baseboard.

16 Component Placement Diagram

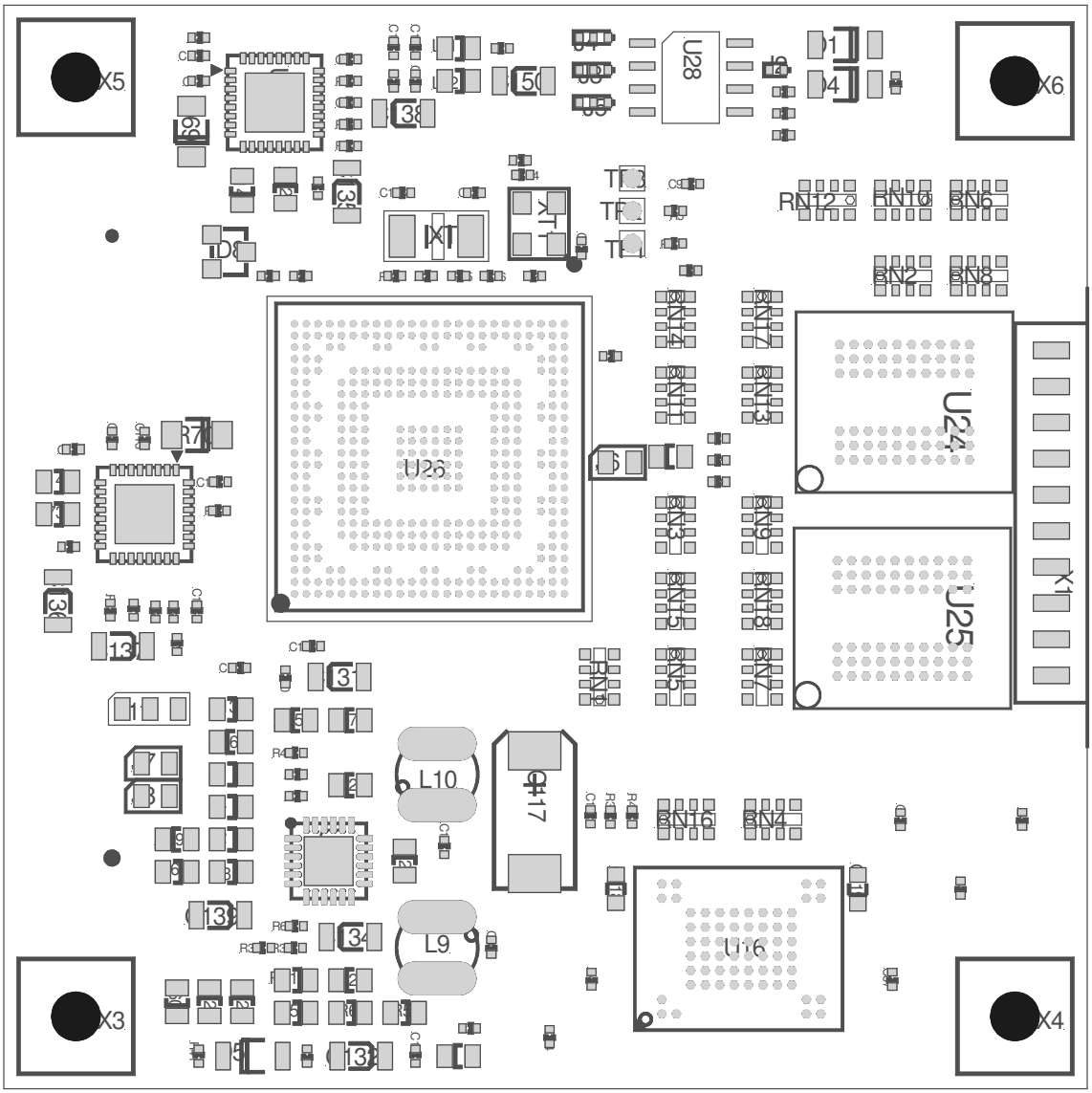


Figure 32: phyCARD-S component placement (top view)

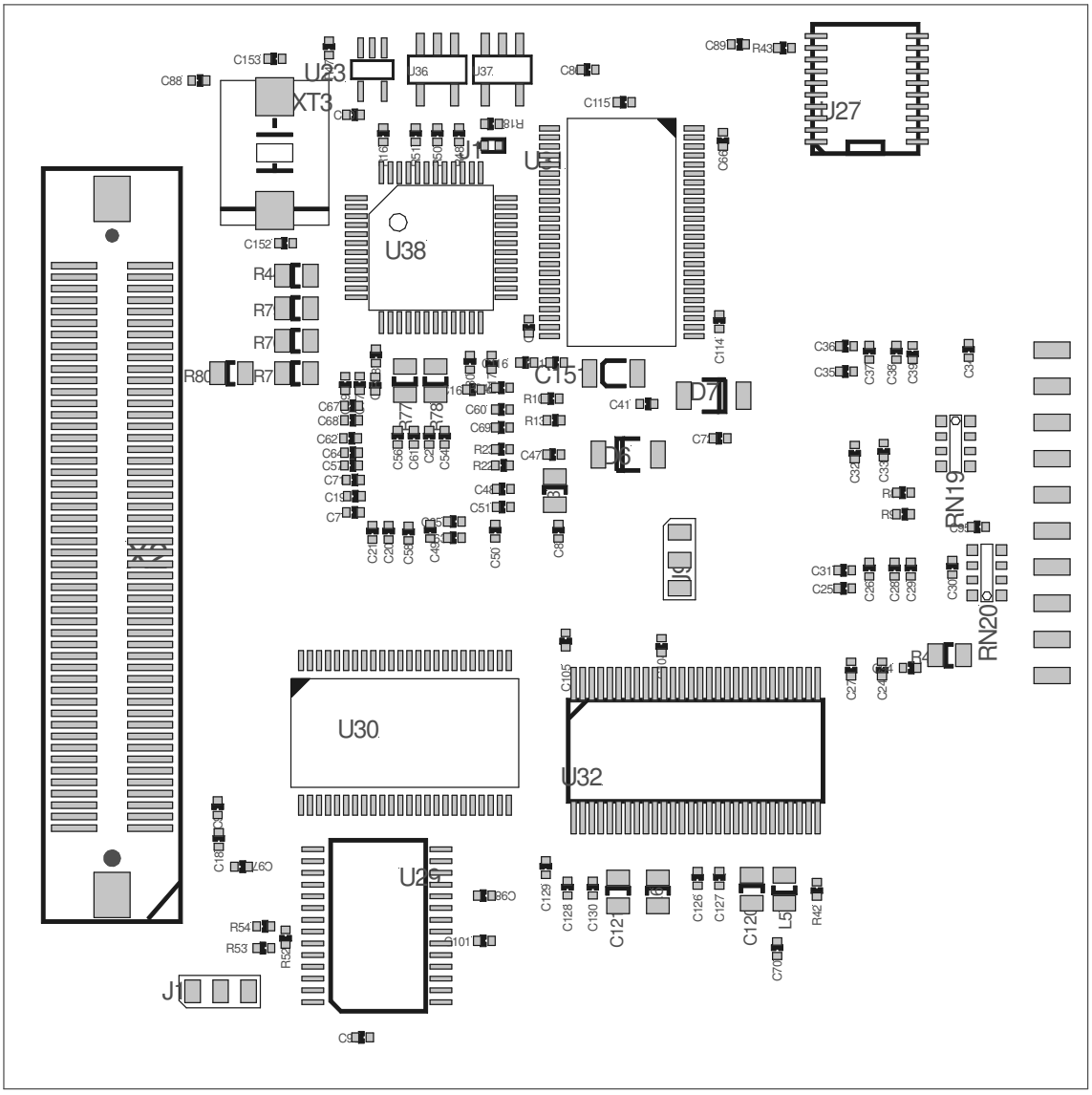


Figure 33: phyCARD-S component placement (bottom view)

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Document:	**phyCARD-S**
Document number:	**L-731e_0, Preliminary Version, July 2009**

How would you improve this manual?

Did you find any mistakes in this manual? page

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Return to:

PHYTEC Technologie Holding AG
Postfach 100403
D-55135 Mainz, Germany
Fax : +49 (6131) 9221-33

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