Purpose: This Product Change Notification (PCN) is to provide notification to PHYTEC customers of component, process or other relevant engineering changes on a PHYTEC hardware subassembly. Impact, qualification, validation and approval of this change shall be documented on the corresponding Customer-Specific Modification (KSM/KSP) form for the PHYTEC hardware subassembly

Product affected / Release Date	
Notice Date: **23.9.2016**	LPN #: **LPN-162e_3**
PHYTEC Subassembly: phyCORE-PXA270	

Standard Product affected	
Date of Change: KW	
PHYTEC Subassembly Part #:	PCM-027
New PHYTEC Part #:	PCM-056 (New subassemblys can be identified via attached version number)

Engineering Change (Component, Firmware, Process, other)		
Current Part		**New Part**
PCM-027	**PHYTEC Internal Part #**	PCM-056
	Manufacturer	
PCM-027	**Manufacturer Part #**	PCM-056
PXA-270	**Description**	PXA-270

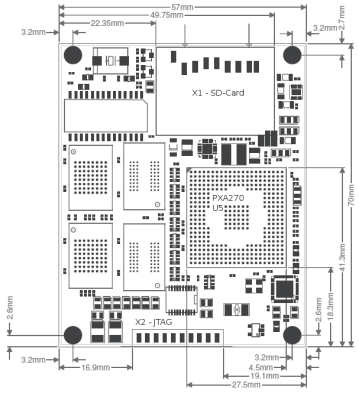
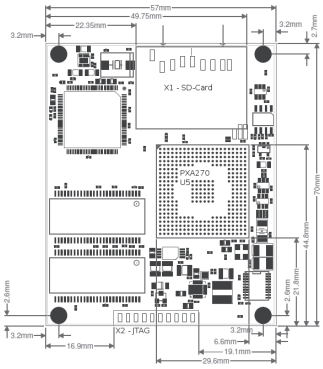
Engineering Change Details
Reason for Component Change: EOL of Micron 256 Mbit SDR(135 nm), Replacement in 55 nm Technology do not run stable on the PCM-027 SOM NRND of ISSI 256 Mbit SDRam (110 nm), Replacement in 63 nm Technology do not run stable on the PCM-027 SOM ==> Redesign of PCB to optimize the Adress-\Data-Bus Routing
Referenced Component Documents:

Impact of Change
(1) no impact in fit and form (2) impact in function

Measures taken by PHYTEC
(1) Redesign the PCB and optimize the Routing for the Adress-\Data- Bus (2) Routing with Impedance of 50 Ohm for the Adress-\Data- Bus (3) Setting Driver Stength for optimum Signal integrity in UBoot to 34.3 Ohm except SDCLK1 (48 Ohm). requirement: PCM-056 with Carrier Board PCM-990

Recommended Measures for Customer
(1) Set the optimum Driver Strength for your Carrier Board in the Uboot (see the patch and Marvell PXA270 Developers Manual on chapter: 6.5.7 Programmable Output Buffer Strength Registers) You have to measure the Signals to set the optimum Driver Strength (2) The Driver Strength after Reset ist 21.8 Ohm. Please integrate the patch for setting the Driver Strength

Technical Differences

Parameter	Original **PCM-027**	Replacement **PCM-056**	**Assess-ment**[1]
Count of Ram Banks	2	1	1
Version with 128 MByte Ram	2 banks with 4 x 32 MByte components	1 bank with 2 x 64 MByte components	1
Dimension and Positions			1
Connector X3	3A = CLKIN_OE 4D/5D = VCC1 6C = VCC_LCD 6D = VCC_BB 9C = VCC_USIM 76C = /CAN_CS0	3A = NC 4D/5D = NC 6C = NC 6D = NC 9C = GND 76C = X_/CAN_CS0	1

[1] Assessments:
1: Effects are to be expected
2: No negative effects are to be expected
3: Better than before
4: Worse than before

Technical Similarities		
Parameter	Original PCM-027	Replacement PCM-056
Version with 64 MByte Ram	1 Ram Bank with 2 x 32 MByte components	
Flash	identical	
Ethernet Controller	identical	
Can-Controlle	identical	
other periphery	identical	

Patch 1 for 64 MByte Ram, Base on U-Boot-2010.09

```
+++ u-boot-2010.09/include/configs/phycore_pxa270.h        2015-01-13 13:20:34.944579026 +0100
@@ -26,8 +26,8 @@
 #ifndef __CONFIG_H
 #define __CONFIG_H

-#define PHYCORE_PXA270_ON_PCM990       0
-#define PHYCORE_PXA270_ON_PCM969       1
+#define PHYCORE_PXA270_ON_PCM990       1
+#define PHYCORE_PXA270_ON_PCM969       0

 #if PHYCORE_PXA270_ON_PCM990 == 1
#include "../../board/phytec/phycore_pxa270/phycore_on_pcm990.h"
@@ -38,7 +38,7 @@
 #endif

 /* Number of installed DRAM banks 1|2 */
-#define CONFIG_NR_DRAM_BANKS   1
+#define CONFIG_NR_DRAM_BANKS   2
@@ -281,6 +281,12 @@
  */
 #define CONFIG_SYS_MDMRS_VAL            0x00020022

+/* BSCNTRx: Programmable Output Buffer Strength Register*/
+#define CONFIG_SYS_BSCTR0_VAL           0x33233333
+#define CONFIG_SYS_BSCTR1_VAL           0x33333353
+#define CONFIG_SYS_BSCTR2_VAL           0x33333333
+#define CONFIG_SYS_BSCTR3_VAL           0x33333333
+

+++ u-boot-2010.09/arch/arm/include/asm/arch-pxa/pxa-regs.h        2014-12-18 09:00:24.384581105 +0100
@@ -2404,6 +2404,10 @@
 #define MCIO0_OFFSET    0x38
 #define MCIO1_OFFSET    0x3C
 #define MDMRS_OFFSET    0x40
+#define BSCTR0_OFFSET   0x4C
+#define BSCTR1_OFFSET   0x50
+#define BSCTR2_OFFSET   0x5C
+#define BSCTR3_OFFSET   0x60

 #define MDCNFG          __REG(0x48000000)  /* SDRAM Configuration Register 0 */
 #define MDCNFG_DE0      0x00000001
```

```
@@ -2428,6 +2432,11 @@
 #define MCI01              __REG(0x4800003C) /* Card interface I/O Space Socket 1 Timing Configuration */
 #define MDMRS              __REG(0x48000040) /* MRS value to be written to SDRAM */
 #define BOOT_DEF           __REG(0x48000044) /* Read-Only Boot-Time Register. Contains BOOT_SEL and PKG_SEL */
+#define BSCTR0             __REG(0x4800004C) /* System Memory Buffer Strength Control Register0*/
+#define BSCTR1             __REG(0x48000050) /* System Memory Buffer Strength Control Register1*/
+#define BSCTR2             __REG(0x4800005C) /* System Memory Buffer Strength Control Register2*/
+#define BSCTR3             __REG(0x48000060) /* System Memory Buffer Strength Control Register3*/

+++ u-boot-2010.09/board/phytec/phycore_pxa270/lowlevel_init.S     2014-12-18 09:00:24.415092078 +0100
@@ -240,7 +240,7 @@
        ldr     r2,     =0xFFF
        bic     r4,     r4, r2

-      /* nimmt den Reset-Wert von MDREFR, löscht DRI und übernimmt DRI aus CONFIG_SYS_MDREFR_VAL */
+      /* nimmt den Reset-Wert von MDREFR, loescht DRI und Uebernimmt DRI aus CONFIG_SYS_MDREFR_VAL */
        ldr     r3,     =CONFIG_SYS_MDREFR_VAL
        and     r3,     r3, r2    /* nur DRI aus CONFIG_SYS_MDREFR_VAL */

@@ -383,6 +383,25 @@
        orr     r3, r3, #MDREFR_APD
        str     r3, [r1, #MDREFR_OFFSET]

+
+      /* BSCTR: Programmable Output Buffer Strength                    */
+      ldr     r2, =CONFIG_SYS_BSCTR0_VAL
+      str     r2, [r1, #BSCTR0_OFFSET]
+      ldr     r2,     [r1, #BSCTR0_OFFSET]
+
+      ldr     r2, =CONFIG_SYS_BSCTR1_VAL
+      str     r2, [r1, #BSCTR1_OFFSET]
+      ldr     r2,     [r1, #BSCTR1_OFFSET]
+
+      ldr     r2, =CONFIG_SYS_BSCTR2_VAL
+      str     r2, [r1, #BSCTR2_OFFSET]
+      ldr     r2,     [r1, #BSCTR2_OFFSET]
+
+      ldr     r2, =CONFIG_SYS_BSCTR3_VAL
+      str     r2, [r1, #BSCTR3_OFFSET]
+      ldr     r2,     [r1, #BSCTR3_OFFSET]
+
```

Additional Patch 2 for 128 MByte Ram

+ use Patch 1 and do the following changes

```
+++ u-boot-2010.09/include/configs/phycore_pxa270.h        2015-01-14 09:30:42.884571234 +0100
@@ -38,7 +38,7 @@
 #endif

 /* Number of installed DRAM banks 1|2 */
 #define CONFIG_NR_DRAM_BANKS    1
@@ -170,7 +170,7 @@
  */
 #define CONFIG_SYS_DRAM_BASE  0xa0000000
 #define CFG_SDRAM_1           0xa0000000      /* SDRAM Bank #1        */
-#define CFG_SDRAM_1_SIZE      0x04000000      /* 64 MB                */
+#define CFG_SDRAM_1_SIZE      0x08000000      /* 128 MB               */

 #if CONFIG_NR_DRAM_BANKS == 2
 #define CFG_SDRAM_2           0xa4000000      /* SDRAM Bank #2        */
@@ -178,7 +178,7 @@
 #endif

 #if CONFIG_NR_DRAM_BANKS == 1
-#define CONFIG_SYS_DRAM_SIZE  0x04000000
+#define CONFIG_SYS_DRAM_SIZE  0x08000000
 #elif CONFIG_NR_DRAM_BANKS == 2
 #define CONFIG_SYS_DRAM_SIZE  0x08000000
 #else
@@ -221,7 +221,7 @@

 #if CONFIG_NR_DRAM_BANKS == 1
 /* K4S561633*/
- #define CONFIG_SYS_MDCNFG_VAL                  0x08000AC8
+ #define CONFIG_SYS_MDCNFG_VAL                  0x88000AD0
```

Note:
Technical differences and similarities in the tables above may not be complete. Please refer to the manufacture datasheets for a complete comparison.

Please contact our support if you need any further information.

Germany and Europe (except France):	**France:**
+49 (6131) 9221-31	+33 (0) 2 43 29 22 33
support@phytec.de	support@phytec.fr
North America:	**India:**
+1 (206) 780-9047, or +1 (800) 278-9913	+91 (80) 4130-7589
support@phytec.com	support@phytec.in