Use of new NOR Flash Parts on phyCORE-i.MX31 (PCM-037)

The information in this document is important and must be followed if you are using phyCORE-i.MX31 SOMs with order code PCM-037-x**0**xxxxxxxx, or corresponding kits (KPCM-...).

Introduction

The NOR Flash parts used on the original design of the PHYTEC phyCORE-i.MX31 System-on-Module were supplied by Intel under the name P33 Strata Flash®. Later, production rights were transferred to Numonyx and subsequently to Micron. The NOR Flash product name also changed to P33 Axcell™ Flash.
In addition Numonyx changed the production process for these components by performing a "die shrink“ to a state-of-the-art 65nm process. Besides a number of changes to the component characteristics and values as depicted in the data sheet there are also new erratas that apply to the current A1 step product revision which need to be taken into consideration

This applies to the following Flash type:

PC28F256P33xF

One of the most significant changes is the 10 ns longer access time. Besides the changes in access timing our component validation investigation found that the new erratas that have been released for this modified Flash part need to be considered. PHYTEC's research has also shown that the errata called "Flexlock Write Timing“ can occur and therefore it is strongly recommended that customers implement the work-around suggested by the component manufacturer Micron.

Micron plans to release a new P33 Flash revision (A2 step) which will fix this errata. Unfortunately market release of this new A2 step has been delayed which forces PHYTEC to use the current A1 step component with all its known erratas and the resulting possible impact on customer applications in order to continue to deliver phyCORE-i.MX31 SOMs.

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The following sections will address the currently known changes identified by PHYTEC and their potential impact on the overall system behavior in conjunction with the phyCORE-i.MX31.

Impact of NOR Flash Change on phyCORE-i.MX31

1. Verification of configured timing values

The NOR Flash on the phyCORE-i.MX31 is accessed via Chip Select Line /CS0. Timing for the memory device selected via /CS0 is done with the help of the CSCR0U, CSCR0L and CSCR0A registers. The recommended register settings for operation with the new P33 NOR Flash (step A1) part are shown in the following tables:

CSCR0U: 0x0000CF03

Field	Reset Value	Recommend Setting
EDC	0x0	0x3
WWS	0x0	0x0
EW	0x0	0x0
WSC	0x1	0xF
CNC	0x0	0x3
DOL	0x0	0x0
SYNC	0x0	0x0
PME	0x0	0x0
PSZ	0x0	0x0
BCS	0x0	0x0
BCD	0x0	0x0
WP	0x0	0x0
SP	0x0	0x0

CSCR0L: 0x10000D03

Field	Reset Value	Recommend Setting
CSEN	0x1	0x1
WRAP	0x0	0x1
CRE	0x0	0x0
PSR	0x0	0x0
CSN	0x0	0x0
DSZ	0x0	0x5
EBC	0x1	0x1
CSA	0x0	0x0
EBWN	0x0	0x0
EBWA	0x0	0x0
OEN	0x0	0x0
OEA	0x0	0x1

CSCR0A: 0x00720900

Field	Reset Value	Recommend Setting
FCE	0x0	0x0
CNC2	0x0	0x0
AGE	0x0	0x0
WWU	0x0	0x0
DCT	0x0	0x0
DWW	0x0	0x0
LBA	0x0	0x1
LBN	0x0	0x2
LAH	0x0	0x0
MUM	0x0	0x0
RWN	0x0	0x2
RWA	0x0	0x7
EBRN	0x0	0x0
EBRA	0x0	0x0

A complete description of these register functions can be found in the Freescale Processor Reference Manual in the following sections:

18.4 Memory Map and Register Definition
18.4.3 Register Descriptions
18.4.3.1 Chip Select *x* Upper Control Register (CSCR*x*U)
18.4.3.2 Chip Select *x* Lower Control Register (CSCRxL)
18.4.3.3 Chip Select *x* Additional Control Register (CSCR*x*A)

2. Implementing the work-around for A1 step errata "Flexlock Write Timing"

Sample source code for implementing this work around in your firmware is available on our FTP server. We also created a modified Linux bootloader which is also available.

PCM-037 Linux:
ftp://ftp.phytec.de/pub/Products/phyCORE-iMX31/Linux/IM590/

PCM-037 WinCE:
ftp://ftp.phytec.de/pub/Products/phyCORE-iMX31/WinCE6.0/IM590/

Summary and Additional Resources

The information in this document has been compiled by PHYTEC to the best of our knowledge. In addition we recommend checking additional documents provided by Micron/Numonyx related to this Flash part revision.

Furthermore it is strongly recommended to perform in-system validation tests using the specific hardware and software environment of your end application.

A complete library of related P33 NOR Flash datasheets, application and errata notes is available on the following URL (as of the time of creating this TechNote):

http://numonyx.com/en-US/MemoryProducts/NOR/Pages/P30P33Documents.aspx

References

Conversion Guide: Numonyx® Axcell™ Flash Memory P33 Stack 256-Mbit/256-Mbit (130nm) to 512-Mbit monolithic (65nm)
Application Note - 309015
Apr 2010

Numonyx® Axcell™ Flash Memory (P33-65nm)
256-Mbit, 512-Mbit (256M/256M)
Datasheet, Order Number: 320003-09
Mar 2010

MCIMX31 and MCIMX31L Applications Processors Reference Manual
MCIMX31RM Rev. 2.4 (12/2008)

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