

miniMODUL-167

Hardware Manual

Edition March 2003

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Preface

This miniMODUL-167 Hardware Manual describes the board's design and functions. Precise specifications for the SABC167 microcontroller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding EMV-Conformity of the PHYTEC miniMODUL-167



PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the EMVG-statute only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC). Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, EMV-Statutes. Only after doing so the devices are allowed to be put into circulation.

The miniMODUL-167 is one of a series of PHYTEC nano-/micro-/miniMODULs which can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit controllers in two ways:

- (1) as the basis for Starter Kits in which user-designed hardware can be implemented on a wrap-field around the controller and
- (2) as insert-ready, fully functional nano-/micro-/miniMODULs which can be embedded directly into the user's peripheral hardware design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. Please contact PHYTEC for additional information.

1 Introduction to the miniMODUL-167

The miniMODUL-167 is an alternative to the PHYTEC miniMODUL-166. It is intended for use in memory intensive applications and operation in a CAN bus system (C167Cx). Furthermore, the module provides a Real-Time Clock that can be battery buffered. An additional UART populates the module, in place of the second asynchronous serial interface of the C166. The miniMODUL-167 enables access to the address and data bus of the C167 controller as well as to 64 free port pins, including 16 analog inputs with 10-bit resolution.

This Hardware Manual describes the features and functions of the miniMODUL-167 (article code MM-311) with the PCB revision #1216.0.

The miniMODUL-167 offers the following features:

- credit card-size dimensions (55 x 85 mm) achieved through modern SMD technology
- improved interference safety through multi-layer technology
- can be plugged into any application like a "big chip"
- requires a single power supply of 5 V₌, typ. < 200 mA
- 16-bit, non-multiplexed bus mode
- 20 MHz CPU speed (100 ns / instruction cycle)
- 16 MByte address space, up to 4 MByte memory on-board
- up to 2 MByte SRAM on-board (up to 1 MByte can be buffered with a battery)¹
- up to 2 MByte Flash memory on-board¹
- on-board Flash programming
- no dedicated programming voltage required through use of 5 V-Flash devices
- up to 2 MByte (EP)ROM on-board¹
- battery buffered RTC-8583 with 256 Byte RAM or RTC-8564
- up to 32 kByte E²PROM or 8 kByte FRAM
- RS-232 transceiver for two serial interfaces
- UART as a second asynchronous serial interface
- provision for operation with in-circuit emulators (ICE/connect 167-interface)

¹: Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

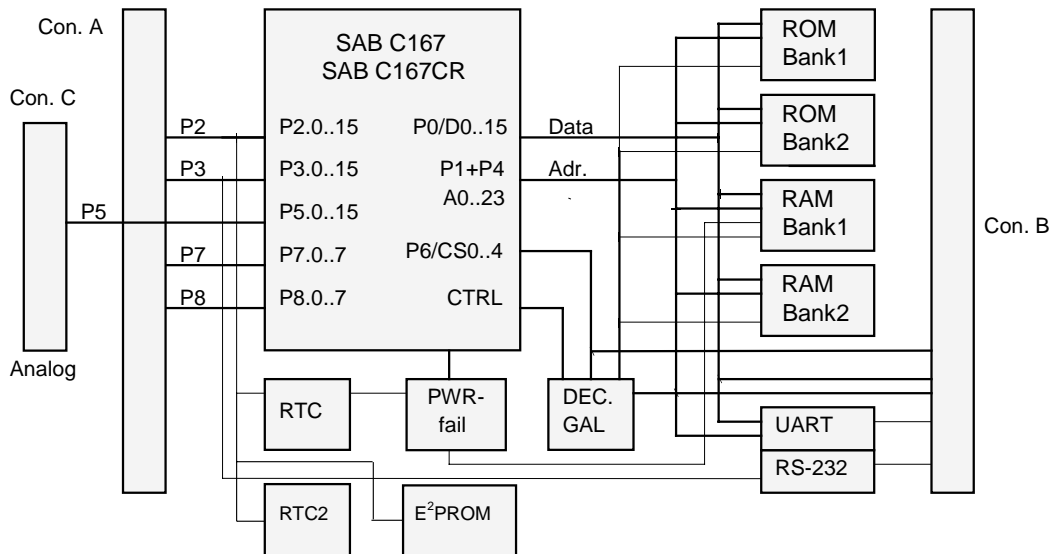


Figure 1: miniMODUL-167 Block Diagram

1.2 View of the miniMODUL-167

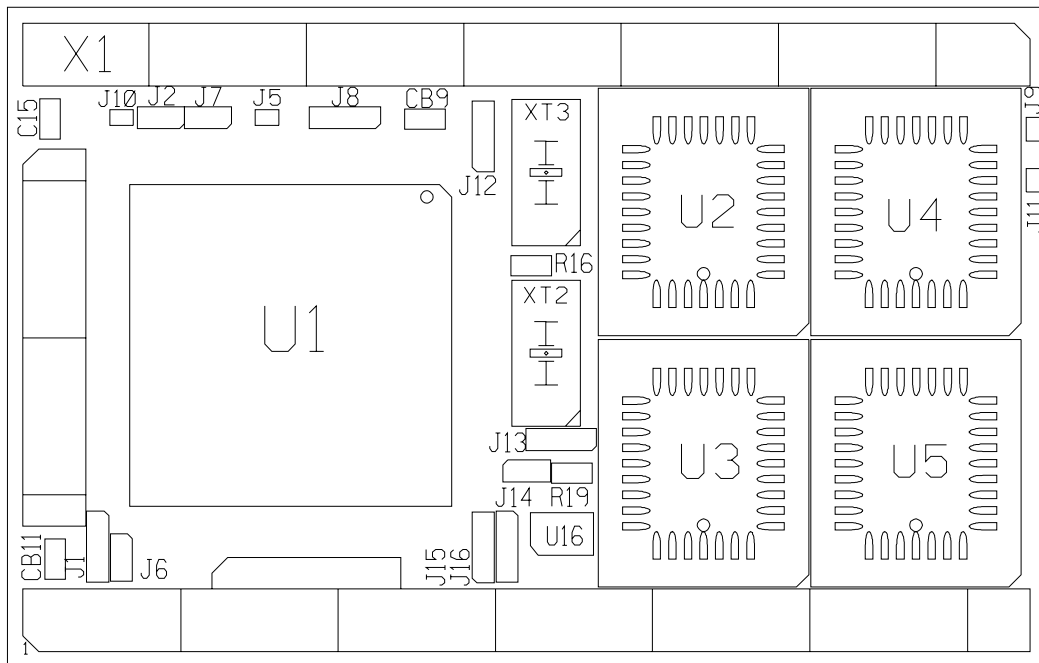


Figure 2: View of the miniMODUL-167 (Top View)

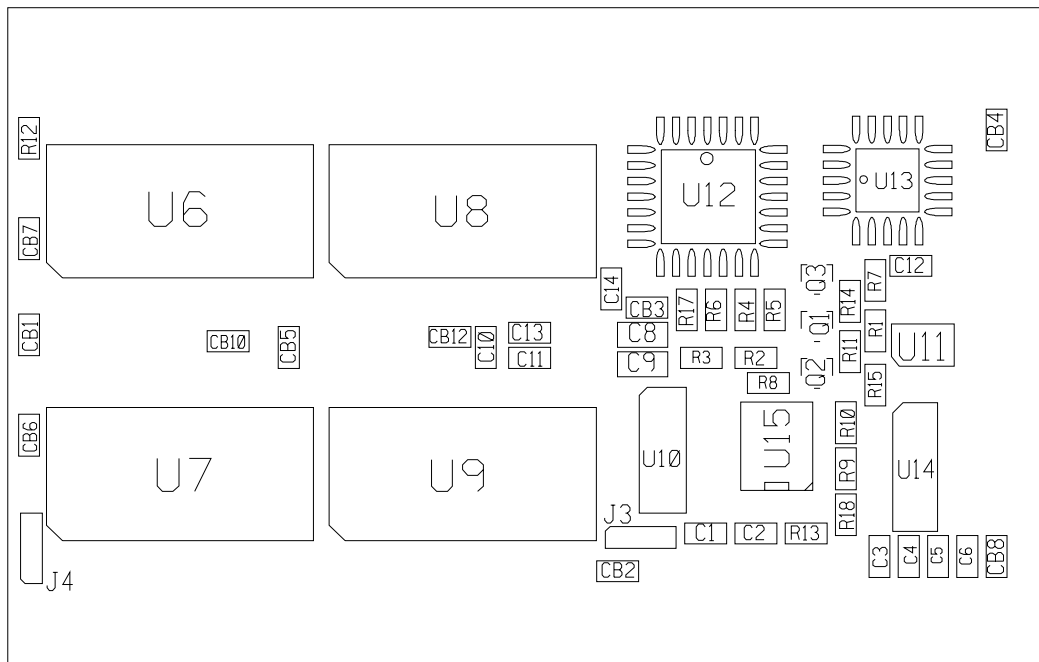


Figure 3: View of the miniMODUL-167 (Bottom View)

2 Pin-Layout

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Caution:

The miniMODUL-167 is based on CMOS technology and, hence, is particularly sensitive to power surges and ESD. Accordingly, unused inputs should be connected to VCC or GND.

The miniMODUL-167 has three pin contact rows (A, B and C) (*refer to Figure 4*) in the form of a dual-rowed socket in a 2.54 mm grid underneath on the circuit board. All relevant signals of the C167 controller, the peripheral hardware and the power supply are connected via these pins. Connector blocks A and B of the module are arranged as two 64-pin connectors along the right and left edges of the module. These connectors include all digital signals with TTL levels, as well as the power supply and RS-232 interface. Contact row C is on the upper edge of the module, running perpendicularly between rows A and B. It is a 24-pin connector. Row C holds all analog signals, assuming that these pins are not used as digital inputs.

A supplemental contact row consisting of six connections is also mounted on the 2.54 mm grid. It is located next to the connector block A pins 14..24. Here the controller signals P4.3..P4.7 (A18..A23 or CAN-RX and CAN-TX) are available.

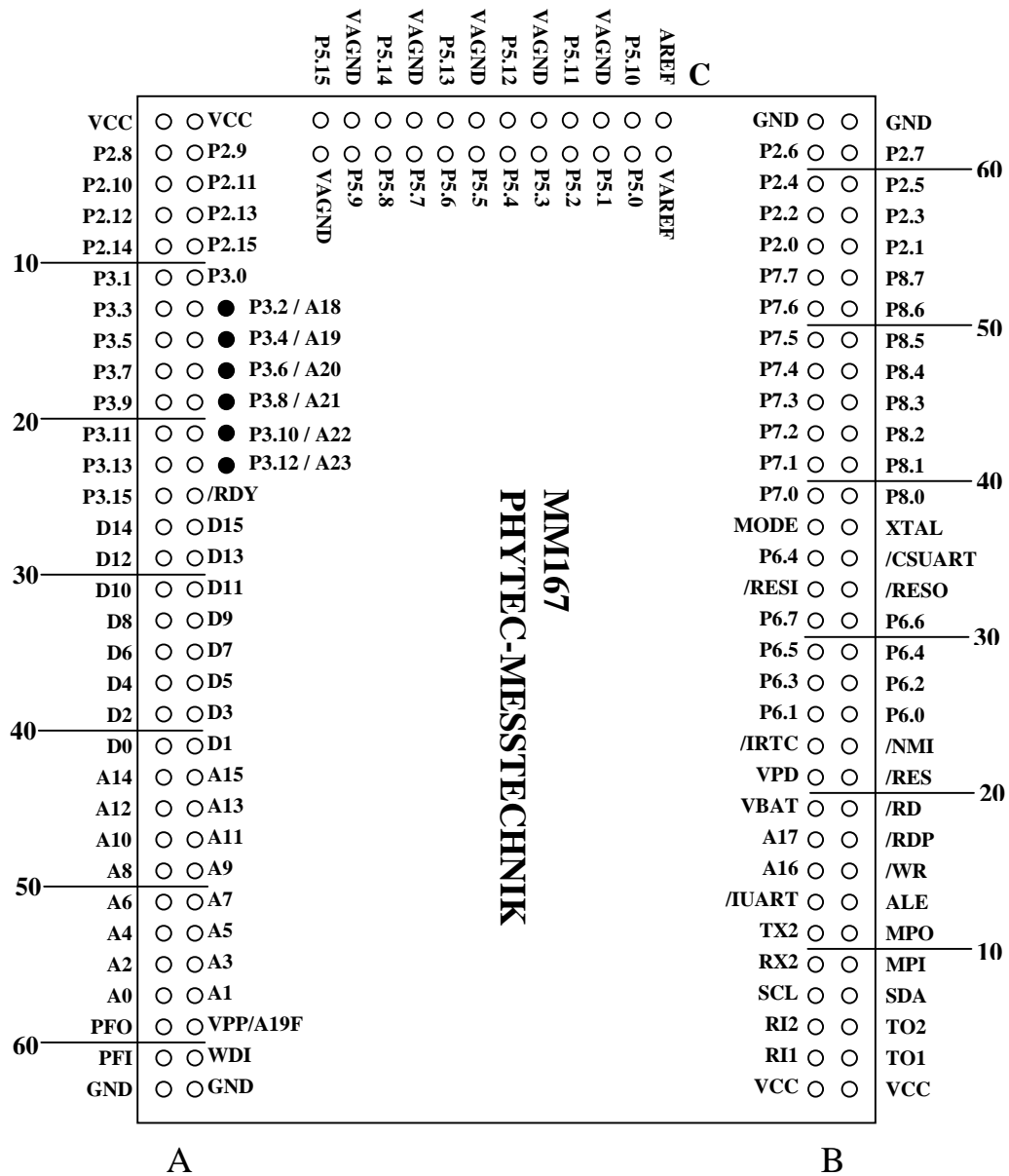


Figure 4: Pin Layout

Table 1 provides an overview of the pin assignments of the miniMODUL-connector.

Row A	Name	Function
A1, A2	VCC	Supply voltage (+5 V +/-5 %, 500 mA)
A3..A10	P2.8..P2.15	C167 high-byte port P2 (refer to C167 User's Manual)
A11, A12 A13, A14 A15, A16 A17, A18 A19, A20 A21, A22 A23, A24 A25	P3.1, P3.0 P3.3, P3.2 P3.5, P3.4 P3.7, P3.6 P3.9, P3.8 P3.11, P3.10 P3.13, P3.12 P3.15	C167 port P3 (refer to C167 User's Manual)
A26	/RDY	C167 /Ready signal input (refer to C167 User's Manual)
A27..A42	D14, D15, D12, D13, D10, D11, ..., D0, D1	C167 port P0 (refer to C167 User's Manual). This line should be connected over a 100 k Ω resistor at Vcc
A43..A58	A14, A15, A12, A13, ..., A0, A1	C167 port P1 (refer to C167 User's Manual)
A59	PFO	MAX690 Power-Fail output (see section "UART, Real-Time Clock, E ² PROM and Battery Buffering" within this manual)
A60	VPP / A19F	Programming voltage input only for 12 V Flash/(EP)ROM devices (U2..U5). This interface should normally remain unconnected.
A61	PFI	MAX690 Power-Fail input (see section "UART, Real-Time Clock, E ² PROM and Battery Buffering" within this manual). If this input is not used, it must be connected to Vcc or GND.
A62	WDI	MAX690 Watchdog input (see section. "UART, Real-Time Clock, E ² PROM and Battery Buffering" within this manual)
A63, A64	GND	Ground connection to the miniMODUL-167 (0 - V).
A65...A70	P4.2...P4.7	C167 port P4.2 to P4.7 carry address lines A18..A23 or the on-chip CAN Interfaces (refer to C167 Derivatives User's Manual)

Row B	Name	Function
B3	TO1	RS-232-level TxD output of the C167 internal asynchronous interface
B4	RI1	RS-232-level RxD input of the C167 internal asynchronous interface
B5	TO2	RS-232-level TxD output of the UART (refer to Philips SCC2691 data sheet)
B6	RI2	RS-232-level RxD input of the UART (refer to SCC2691 data sheet)
B7	SDA	RTC Data lines of the I ² C Bus (refer to RTC data sheet)
B8	SCL	RTC Clock lines of the I ² C bus (refer to RTC data sheet)
B9	MPI	UART multipurpose input (refer to SCC2691 data sheet)
B10	RX2	UART RxD input (TTL levels of the RI2 inputs of the RS-232 interface)
B11	MPO	UART multipurpose input (refer to SCC2691 data book)
B12	TX2	UART TxD output (TTL levels of the TO2 output of the RS-232 interface)
B13	ALE	C167 ALE signal output (refer to C167 User's Manual)
B14	/IUART	UART /Interrupt output (open drain)
B15	/WR	C167 /WR signal output (refer to C167 User's Manual)
B16, B18	A16, A17	C167 port P4.0, P4.1 (refer to C167 User's Manual)
B17	/RDP	C167 /RD signal output (refer to C167 User's Manual)
B19	/RD	/RD-signal-input for memory devices of the module (connected via J11 with /RDP)
B20	VBAT	Battery input for backup of RAM and RTC (see section 5.3, "Battery-Backup/Reset" of this manual).
B21	/RES	MAX690 /RESET output (open drain)

Row B	Name	Function
B22	VPD	Output of the backup voltage (Vcc/VBAT) for buffering external components.
B23	/NMI	C167 /NMI output (<i>refer to C167 User's Manual</i>). This input must be connected with a Pull-up-resistor at Vcc.
B24	/IRTC	RTC /Interrupt output (open drain)
B25..B32	P6.0..P6.7	C167 port P6 (<i>refer to C167 User's Manual</i>). P6.0..P6.4 is used for controller-internal /Csx-signals from the module (<i>refer to the section 4, "Memory Models" in this manual</i>).
B33	/RESO	C167 /RESOUT signal (Reset output) (<i>refer to C167 User's Manual</i>).
B34	/RESI	C167 /RESIN signal (Reset input) (<i>refer to C167 User's Manual</i>), connected to /RES by default
B35	/CSUART	UART /Chip Select-input (typically connected via J7 with P6.4 = /CS4 of the controller).
B36	P6.4	C167 /CS4 signal allowing compatibility with the PHYTEC miniMODUL-166 on this pin.
B37	XTAL	C167 XTAL1 signal output (<i>refer to C167 User's Manual</i>).
B38	MODE	Mode input of the decoder GAL (allowing the selection of a second memory model)
B39, B41,..B53	P8.0..P8.7	C167 port P8 (<i>refer to C167 User's Manual</i>)
B40, B42, ..B54	P7.0..P7.7	C167 port P7 (<i>refer to C167 User's Manual</i>)
B55..B62	P2.1, P2.0, P2.3, ..., P2.7, P2.6	C167 low byte port P2 (<i>refer to C167 User's Manual</i>)
B63, B64	GND	Ground connection of the miniMODUL-167 (0 V)

Row C	Name	Function
C1, C2	VAREF	C167 reference voltage input (+5 V, refer to C167 User's Manual)
C5, C9, C13, C17, C21,C24	VAGND	C167 analog ground input (0 V, refer to C167 User's Manual). Must be connected to GND-potential.
C4, C6, C8, C10, C12, C14, C16, C18, C20, C22 C3, C7, C11, C15, C19, C23	P5.0, P5.1, P5.2, P5.3, P5.4, P5.5, P5.6, P5.7, P5.8, P5.9 P5.10, P5.11, P5.12, P5.13, P5.14, P5.15	C167 port P5 analog input (0 to 5 V/10-bit, refer to C167 User's Manual)

Table 1: Pinout of the miniMODUL-Connectors

2.1 ICE/Connect-167

When implementing the ICE/connect-167 interface (available from HITEX Development Tools, <http://www.hitex.com>), the following signals can be accessed at the pin header rows of the miniMODUL-167:

Interface	Pins
P0.0 - P0.15 = D0...15	A27..A42
P1.0 - P1.15 = A0...15	A43..A58
P4.0 - P4.7 = A16...A23	B16, B18, A65..A70
P6.0 - P6.4	B25..B29
ALE	B13
XTAL1	B37
/WR	B15
/BHE = P3.12	A24
/HLDA = P6.6	B31
+5 V = Vcc	A1, A2, B1, B2
GND	A63, A64, B63, B64

Table 2: Pinout of the ICE/Connect-167

Several signals must be linked through the emulator. Unused signals can be disregarded.

Interface	Explanation	Pin
/RSTIN-P = /RESI	/RESIN-Controller	B34
/RSTIN-U = /RES	/RESIN-Environment	B21
/NMI-P = /NMI	/NMI-Controller	B23
/RD-P = /RDP	/RD-Controller	B17
/RD-U = /RD	/RD-Environment	B19
/RSTOUT-P = /RESO	/RESOUT-Controller	B33
/READY-P = /RDY	/READY-Controller	A26
/HOLD-P = P6.5	/HOLD-Controller	B30

Only the following signals are utilized on the miniMODUL-167 in conjunction with the ICE/connect-167:

Interface	Pin
/RSTIN-P, /RSTIN-U	B34 and B21, can be separated with J5
/RD-P, /RD-U	B17 and B19, can be separated with J11

We recommend using the HITEX adapter board to connect the PHYTEC miniMODUL-167 to the ICE/connect-167.

3 Jumper

For configuration purposes, the miniMODUL-167 has 16 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 2* and *Figure 3* indicate the location of the jumpers on the board.

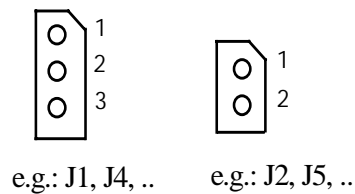


Figure 5: Numbering of the Jumper Pads

3.1 J1 Internal or External Program Memory

At the time of delivery, Jumper J1 is closed at 2+3. This default configuration means that the program stored in the external program memory is executed after a hardware reset. In order to allow the execution of a specific controller's internal program memory, Jumper J1 must be closed at 1+2.

The following configurations are possible:

Code Fetch Selection	J1
Execution from external program memory	2 + 3*
Execution from internal program memory	1 + 2

* = Default setting

Table 3: J1 Code Fetch Selection

3.2 J2 Connection Pin A23 (P3.13) with /WR Signal

J2 produces a connection between pin A23 (P3.13) and the /WR signal of the controller. With this, the pin compatibility of pin A23 to the miniMODUL-166 can be made. In such a case, port P3.13 may not be initialized as an output (which is also true of the miniMODUL-166). Normally this jumper is open, hence P3.13 of the C167 is fully functional.

The following configurations are possible:

Pin A23 and /WR-Signal	J2
Pin A23 = P3.13 (standard)	open*
Pin A23 = /WR (pin compatible with MM-166)	closed

* = Default setting

Table 4: J2 Connection Pin A23 (P3.13) with /WR Signal

3.3 J3 Use of Pin 30 on the SRAM

Jumper J3 determines the use of pin 30 on the SRAM devices at U6/U7 or U8/U9. This jumper is configured at time of delivery of the module and must not be changed by the user.

The following configurations are possible:

SRAM Configuration	J3
128 kByte SRAM per device (256 kByte / bank)	1 + 2
512 kByte SRAM per device (1 MByte / bank)	2 + 3

Table 5: J3 SRAM Capacity Configuration

3.4 J4 Flash Pin 1 Configuration

J4 enables selection of the installed Flash/(EP)ROM chips on U2/U3 and/or U4/U5, so that address line A19 of the controller or the Vpp-input of the miniMODUL-167 can be connected at pin 1 of the memory device.

The following configurations are possible:

Flash Pin 1	J4
VPP for 12 V Flash-/(EP)ROM types up to 128k x 8-bit per device	1 + 2
A19 for Flash-EPROM 512k x 8-bit per device (1 MByte / bank)	2 + 3

Table 6: J4 Flash Type and Size Configuration

3.5 J5 Reset Signal Configuration

J5 separates the reset signal of the miniMODUL-167 (/RES) from the RESET input (/RESI) of the controller. Thus both signals are separated and available at pins B21 = /RES and B34 = /RESI and can be driven by in-circuit emulators (such as the ICE/connect-167 interface of HITEK Development Tool's T32 and AX166 emulators). This jumper is closed in normal operation.

The following configurations are possible:

Reset-Signal	J5
Reset signal /RES of the module connected with mit Reset input (/RESI) of the controller	closed*
/RES and /RESI available at B21 and B34 separately	open

* = Default setting

Table 7: J5 Reset Signal Configuration

3.6 J6 Serial Interface Configuration

J6 connects the asynchronous serial interface (P3.11 = RxD) of the C167 with the RS-232 transceiver on the miniMODUL-167. By opening this jumper, connection of the TTL level signal to other transceiver devices is possible. The controller port can also function as standard I/O port. Typically, this jumper is closed, hence configuring an RS-232 interface available at pins B3 and B4 of the miniMODUL-167 connector.

The following configurations are possible:

Configuration of P3.11	J6
P3.11/RxD connected to on-board RS-232 transceiver	closed*
P3.11 as I/O pin or RxD with TTL level	open

* = Default setting

Table 8: J6 Serial Interface Configuration

3.7 J7 /CS4 Configuration

J7 separates the connection between the /CS4 output of the controller and the chip select input (/CSUART) of the external UART (SCC2691) on the miniMODUL-167. With this, the UART can be addressed without further external address decoding from the controller. This jumper is closed upon delivery of the board. Should the user open this jumper, the /CS input of the UART (B35) must be connected to VCC, or controlled by another /CS signal.

The following configurations are possible:

Use of /CS4 as /CSUART	J7
/CS4 from the controller as /CS for UART	closed*
P6.4 (/CS4) disconnected from /CSUART	open

* = Default setting

Table 9: J7 /CS4 Configuration

3.8 J8 RTC and UART Interrupt Outputs

J8 connects the interrupt outputs from the RTC and UART to port pin P2.0 of the controller. With this, both devices with their open-drain outputs can release an active-low interrupt at port P2.0 of the controller. With Jumper J8 closed in position 1+2, the interrupt output of the external UART (SCC2691) is connected to port P2.0 of the controller. If the jumper is closed in position 2+3, the RTC can release an interrupt on port P2.0. Both signals can also be combined with each other (J8: 1+2+3). In this case, the source of the interrupt must be queried by software via the status register of the RTC or the UART.

The following configurations are possible:

Interrupt-Quelle an P2.0	J8
P2.0 used as port pin, no interrupt source connected	open *
UART interrupt connected with P2.0	1 + 2
RTC interrupt connected with P2.0	2 + 3
UART and RTC interrupt connected with P2.0	1 + 2 + 3

* = Default setting

Table 10: J8 P2.0 Configuration, Interrupt Sources

3.9 J9, J10 Configuration of P2.1, P2.2 for I²C Bus

J9 and J10 can be used to separate the I²C bus signals from the port pins P2.1 and P2.2. The I²C bus of the RTC/E²PROM is already connected to ports P2.1=SCL and P2.2=SDA on the miniMODUL-167. If these port pins are required for other functions, port P2.1 can be separated from SCL with Jumper J9. Opening J10, port P2.2 can likewise be separated from SDA of the RTC/E²PROM. In order to use the RTC/E²PROM in such a configuration, an external connection must be made between other ports and the signals SCL and SDA. The driver software for the I²C functions must also be adapted accordingly.

The following configurations are possible:

Port P2.1 and P2.2 Configuration	J9	J10
Port P2.1 as I/O pin at pin B57	open	
Port P2.1 as I ² C SCL	closed*	
Port P2.2 as I/O pin at pin B58		open
Port P2.2 as I ² C SDA		closed*

* = Default setting

Table 11: J9, J10 I²C Bus Configuration

3.10 J11 /RD Signal Connection

J11 separates the connections between B17 and B19 on the miniMODUL-167. This jumper connects the /RD signal of the controller (/RDP) with the /RD signal of the module. This connection can be opened to connect an emulator (ICE/connect-167) to the board. In order to operate the module without an emulator, both signals must be connected.

The following configurations are possible:

Connection between /RDP and /RD	J11
/RD signal of the controller (/RDP) connected with /RD signal (/RD) of the module	closed*
/RDP disconnected from /RD	open

* = Default setting

Table 12: J11 /RD Signals Connection

3.11 J12 GAL Inputs Selection for Address Decoding

J12 selects the GAL inputs used for address decoding. In the standard configuration of the miniMODUL-167, P6.3 (J12 = 1+2) is connected to GAL, which enables flexible address decoding with /CS signals of the controller for all four memory banks (*refer to section 4, "Memory Model MODE = 1"*). As an alternative, with J12 = 2+3, the address line A21 can be connected to the GAL device, whereby address decoding for up to 4 MByte address space is possible without controller-internal /CS signals (MODE = 0).

The following configurations are possible:

GAL Input	J12
P6.0...3 = /CS0..3 for 4 memory banks (MODE = 1)	1 + 2*
A21 connected to GAL, enables decoding of 4 memory banks with address signals in the GAL (/CS1...3 of the C167 freely available)	2 + 3

* = Default setting

Table 13: J12 Address Decoder Input Configuration

3.12 J13 E²PROM/FRAM Supply Voltage

The device at U16 can be connected to VCC or VPD using Jumper J13. As default, U16 is populated with a serial E²PROM with voltage supply pins connected to VCC. Alternatively, a serial FRAM device can also populate U16, in order to support frequent write cycles, for instance. If mounted with an FRAM device, the circuit supply pins can be applied to the battery voltage VPD for purposes of data buffering.

The following configurations are possible:

Supply Voltage for U16	J13
E ² PROM/FRAM at U16 supplied with VCC	1 + 2*
E ² PROM/FRAM at U16 supplied with VPD	2 + 3

* = Default setting

Table 14: J13 E²PROM/FRAM Supply Voltage Configuration

3.13 J14 Write Protection of E²PROM/FRAM

Various types of E²PROM/FRAM can populate space U16. Some of these devices provide a write protection function¹. Closing Jumper J14 connects pin 7 of the serial E²PROM/FRAM with VCC and thus activates write protection.

The following configurations are possible:

Write Protection E²PROM/FRAM	J14
Write protection of E ² PROM/FRAM deactivated	open*
Write protection of E ² PROM/FRAM activated	closed

* = Default setting

Table 15: J14 Write Protection of E²PROM/FRAM

3.14 J15, J16 Address of the Serial E²PROM/ FRAM

Jumper J15 and J16 configure the serial E²PROM/FRAM address. The default configuration sets the address to 0xA8.

The following configurations are possible:

Address E²PROM/FRAM	J15	J16
0xA0	1 + 2	2 + 3
0xA4	2 + 3	2 + 3
0xA8	1 + 2*	1 + 2*
0xAC	2 + 3	1 + 2

* = Default setting

Table 16: J15, J16 E²PROM/FRAM Address Configuration

¹: Refer to the corresponding E²PROM/FRAM Data Sheet for more information on the write protection function.

4 Memory Models

The C167 microcontroller provides up to five Chip Select outputs (/CS0 to /CS4) which, can be initialized by software and assigned to various address areas during run time of the controller. This extremely flexible concept is expanded through a supplementary address decoder in the form of a GAL16V8-device on the miniMODUL-167. By configuring the MODE input of the miniMODUL-167, one of two memory models can be chosen. Setting MODE to 1, the /CS signals for the various memory devices are derived from the internal /CS signals and the A0 and /BHE signals. This means that the memory model is defined through the controller-internal mechanism by means of SFR ADDRSEL_x and BUSCON_x. Setting MODE to 0, the memory model programmed in the GAL is chosen. Address decoding is done with address lines A18 to A21, without the controllers /CS signals, hence making these signals available as port connections for external digital extensions.

Caution:

Use of memory devices larger than 1 MByte, requires the corresponding segment address lines of the controller to be activated via configuration resistors at P0H.3 and P0H.4 (D11, D12) that are fetched during Reset (*refer to Table 17*).

The memory model of the standard GAL has the following functions:

MODE = 1:	/CS0	=	ROM-Bank 1,
	/CS1	=	RAM-Bank 1,
	/CS2	=	RAM-Bank 2,
	/CS3	=	ROM-Bank 2.

In this mode the SFR ADDRSEL_x and BUSCON_x define the address areas for /CS0, /CS1, /CS2 and /CS3. As the memory model is defined by software this is a very flexible model. It is especially suitable for development using a debugger software development tools, as the program includes the software for configuring the memory model.

Following a reset, only the /CS0 connection is available for accessing the entire address area of the controller (in MODE = 1, ROM-Bank-1 = U2/3). /CS0 is always active in those areas in which no other /CSx-signals are active. To access additional /CSx-signals of the C167, the corresponding ADDRESELx register must be configured for the desired address area. Only after doing this, the BUSCONx-register can be configured in order to activate the corresponding /CSx-signal.

Note that no /CSx-signals must overlap and that the area of the program code within /CS0 cannot be superceded by another /CSx-signal.

MODE = 0: /CS0 + /A18+ /A19 = ROM-Bank 1, (256 kByte)
 /CS0 + A18 + /A19 = RAM-Bank 1, (256 kByte)
 /CS0 + /A18 + A19 = RAM-Bank 2, (256 kByte)
 /CS0 + A18 + A19 = ROM-Bank 2, (256 kByte)

This alternate model (MODE = 0) is especially suitable for final operation with the finished software in the Flash memory. Since the internal address-decoder of the controller is not used, the only delay time occurring is that of the GAL between the address signals of the controller and the activation of the Chip Select signals of the memory chips. The /CS signals of the C167 (/CS0.../CS4) can be used for external connection to the miniMODUL-167.

Two examples for configuring the memory of the miniMODUL-167 are provided below.

a) Configuration: MODE = 1 (controller-internal /CS signals)

ADDRSEL1 = 0406h: /CS1 4:000-7:FFFFh (256 kByte RAM-1)
ADDRSEL2 = 0806h: /CS2 8:000-B:FFFFh (256 kByte RAM-2)
ADDRSEL3 = 0C06h: /CS3 C:000-F:FFFFh (256 kByte ROM-2)
ADDRSEL4 = 1000h: /CS4 10:000-10:0FFFh (4 kByte UART)

BUSCON0 = 04AEh Bus active for /CS0 (ROM-Bank-1)
BUSCON1 = 04AEh Bus active for /CS1 (RAM-Bank-1)
BUSCON2 = 04AEh Bus active for /CS2 (RAM-Bank-2)
BUSCON3 = 04AEh Bus active for /CS3 (ROM-Bank-2)
BUSCON4 = 060Dh Bus active for /CS4 (UART)

b) Configuration: MODE = 0 (external /CS signals from GAL)

BUSCON0 = 04AEh, BUSCON1..4 = 0000h CS1.../CS4 not active

Segment addresses A16..A19 must be activated (P0H3 = d11 = 0)!

These memory models are illustrated in the following diagram:

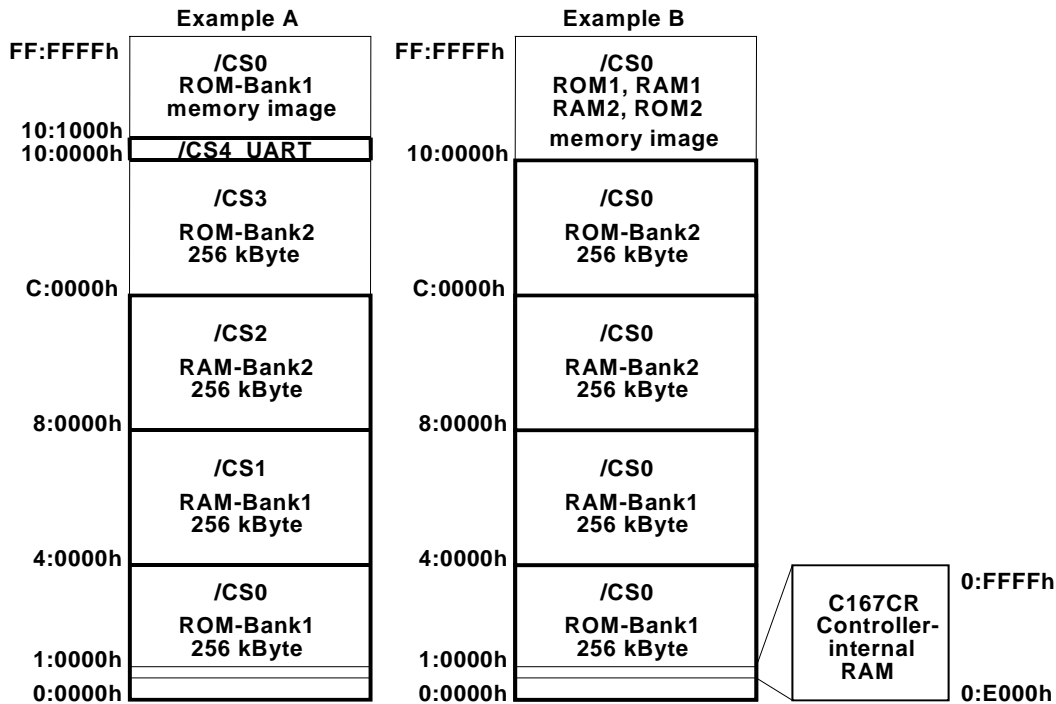


Figure 6: Memory Models

4.1 Bus-Timing

For connecting additional peripheral hardware the boards recommended values for the BUSCONx registers are:

BUSCONx: 04AEh = 1 wait states, R/W delay, no tri-state short ALE, 16-bit de-multiplexed, address-/CSx, active (for memory devices running up to 70 ns on the miniMODUL-167)

This configuration uses one wait state and the R/W delay. When using one wait state (Tc = 50 ns) and the R/W delay, all memories must respond within an access time of 70 ns at a bus cycle time of 150 ns.

In order to be able to use the controller without wait states, decoding must be executed only with the external GAL (16V8-10). In this case, the controller's internal /CS signals must remain unused and memories with a maximum of 55 ns access time are required on the module.

Note:

At the moment, the miniMODUL-167 is equipped with a 70 ns Flash memory and a 70 ns RAM. This configuration only allows operation with a minimum of one wait state and R/W delay.

Important signal times in 16-bit bus non-multiplexed mode at 20 MHz clock frequency (F_{osc}) are:

- $T_c = 50 \text{ ns} \times \text{wait state control (MCTC in BUSCON)}$
- $T_f = 50 \text{ ns} \times \text{tri-state control (MTTC in BUSCON)}$

- Addresses stable for valid data max. $\text{max } 70 \text{ ns} + T_c \text{ SR}^1$
- /RD low for data valid max $\text{max } 55 \text{ ns} + T_c \text{ SR}^1$
- /RD low for data valid (/R/W delay) $\text{max } 30 \text{ ns} + T_c \text{ SR}^1$
- /RD high for data bus high-Z $\text{max } 15 \text{ ns} + T_f \text{ SR}^1$
- /RD high for data high-Z (R/W delay) $\text{max } 35 \text{ ns} + T_f \text{ SR}^1$
- /CS for data valid $\text{min } 55 \text{ ns} + T_c \text{ SR}^1$
- /RD and /WR low $\text{min } 65 \text{ ns} + T_c \text{ CC}^2$
- /RD and /WR low (R/W delay) $\text{min } 40 \text{ ns} + T_c \text{ CC}^2$
- /WR low for data valid $\text{min } 25 \text{ ns} + T_c \text{ CC}^2$
- /WR high for data invalid $\text{min } 15 \text{ ns} + T_f \text{ CC}^2$

¹ SR = System request: requests must be kept from switching the C167

²: CC = Controller characteristic: the controller guarantees these times for turn-off

5 Hints for Handling the the miniMODUL-167

5.1 Connecting External Circuitry

Any 167-derivative controller (C167CR, C167CS, etc.) can be populated on the miniMODUL-167. Please note that when using the on-chip CAN interface, only 20 external address lines (A0...A19), and hence 1 MByte of associated address space per /CSx signal, is available. By using all /CS connections, a maximum of 5 MByte can be addressed. If address lines A18..A23 are used, a port 0 configuration resistor (e.g. 4k Ω to GND) at P0H3 is necessary.

Address and data buses extend from the controller to the pin headers at the edges of the board without any buffer. When connecting external chips to the data/address bus as well as to the control lines (/RD, /WR), the user should provide external buffers (such as the 74AHCT245) to these signals between the module and the peripheral devices.

The data bus D0..15 (port 0) should be attached to the VCC through a 100 k Ω pull-up-resistor. You should provide for the possibility of attaching pull-down resistors directly to port 0 (pin 0..15) to set the processor configuration. This enables start of the C167 in different configurations, as these pins are read during reset (*refer to the C167 User's Manual*). Such a resistor is already provided on the miniMODUL-167 at port POL.6, allowing the non-multiplexed mode for the data/address bus to be set. The user must provide an additional resistor via a jumper at port POL.4 to enable the C167 to start by means of the internal Bootstrap Loader. This allows the chip-internal Bootstrap Loader to be started each time by closing a jumper. This is necessary, for instance, when programming a Flash memory from software updates or when downloading an application program via the FlashTools download utilities. A Monitor program can also be started via the Bootstrap Loader.

P0 Configuration Functions (* = module standard configuration)

Port Pin	Function, if R = 4.7k to GND	Read at:
P0L.0	Emulation Mode	Hardware-Reset
P0L.1	Adapt Mode (ONCE mode)	Hardware-Reset
P0L.4	Bootstrap Loader Mode	Hardware-Reset
P0L.6	* - Bus Mode (Non-Multiplexed)	HW-/SW- Reset
P0L.7	Data-bus width (8-bit Data bus)	HW-/SW- Reset
P0H.1 P0H.2	Number of /CSx signals at port P6 * - P0H2, P0H1 = 1, 1 = 5 (/CS0../CS4) P0H2, P0H1 = 1, 0 = 0 (no /CS) P0H2, P0H1 = 1, 1 = 2 (/CS0, /CS1) P0H2, P0H1 = 1, 0 = 3 (/CS0../CS2)	HW-/SW- Reset
P0H.3 P0H.4	Number of segment address lines on port P4 * - P0H4, P0H3 = 1, 1 = 2 (A16, A17) P0H4, P0H3 = 1, 0 = 8 (A16..A23) P0H4, P0H3 = 0, 1 = 0 (no /CS) P0H4, P0H3 = 0, 0 = 4 (A16..A19)	HW-/SW- Reset
P0H.5 P0H.6 P0H.7	Clock mode / PLL factor (not available on all C167 controllers)	HW-/SW- Reset

Table 17: Configuration of the Controller via P0

For additional information on P0 configuration functions, refer to the C167 User's Manual.

The NMI input should have a pull-up resistor (10 K) to VCC. The NMI can thus be released with a falling edge (e.g. with a push button to Ground) which is useful in software development via a Monitor program.

Do not connect the VPP pin to a 12 V power source given the standard configuration of the miniMODUL-167, which is populated with 5 V Flash memory devices (either type 29F010 or 29F040 from AMD).

If a larger memory device (>1024 x 8) populates the module, or if the memory model MODE = 0, the upper segment addresses A19...A23 must be made available by connecting port P0H.3 with a 4k7 Ohm resistor to GND.

5.2 Memory Access Times and Memory Configuration

The standard miniMODUL-167 operates in a 16-bit non-multiplexed mode and uses the signals A0 and /BHE for bus access (generated by the chip) to the low- and high-bytes in the memory. This also allows memory access by byte access.

At memory banks U2/U3 and U4/U5, Flash devices of 256k x 8 to 4096k x 8 capacity in PLCC32 housing can be populated. Pin-compatible (EP)ROM devices (1024k x 8 to 2048k x 8) can also be mounted on the same shapes. U2/U3 represents the first ROM bank. U4 and U5 comprise the second ROM bank. U6 and U7 are designated as the first RAM bank and can be populated with 1024k x 8 or 4096k x 8 SRAM in SO32 housing. This RAM bank can be buffered via an external battery. U8/U9 form the second RAM bank and can be populated with memory chips similar to those used in U6/U7.

Please note the maximum controller speed cannot be attained with the chips currently installed on the miniMODUL-167. In view of the timing of the controller and the 70 ns access capability of the Flash memory (and RAM), we recommend that the user program one wait state and one R/W delay in the corresponding BUSCONx registers. The /CS signals that control the on-board memory devices internal Chip Select signals (P6.0..3) are used. These /CS signals have a delay time of about 20 ns compared to the address signals. If the user desires to run very quick software routines, then these routines should be run out of a RAM bank on the module (one wait state). An alternate is to do the address decoding (Chip Select signals) exclusively via the GAL (max. 10 ns) and to install faster memory chips (Flash and RAM with max. 55 ns) on the module.

In the standard memory configuration (MODE =1) of the miniMODUL-167, the first Flash memory bank is addressed with the /CS0 signal of the controller; /CS1 selects the module's first RAM bank and the second RAM bank is enabled via the /CS2 of the controller. /CS3 accesses the second Flash-EPROM bank. /CS4 controls the UART (SCC2691).

In MODE = 0 on the miniMODUL-167, memories are only selected through the address lines of the controller (A18..A23) and through the /CS0 signal (*refer to section 4, "Memory Models" of this manual*).

5.3 UART, Real-Time Clock, E²PROM and Battery Buffering

The external UART (additional serial interface of the miniMODUL-167) is selected via the controllers Chip Select signal /CS4 on port P6.4 (*refer to section 3.7*). The UART chip can only be addressed in 8-bit mode, configuration: BUSCON4 = 060Dh (8-bit demultiplexed, R/W delay, tri-state wait, long ALE, two wait states). A driver for the operation of the chip is supplied on the enclosed Spectrum CD included with the miniMODUL-167. The interrupt output (open-drain) of the UART (/IUART = PIN B14) can be routed to port P2.0 of the controller with Jumper J8 (*refer to section 3.8*).

The RTC and E²PROM are addressable via the port pins P2.1 = SCL and P2.2 = SDA, using the I²C bus protocol. The interrupt output of the RTC can also be connected to port P2.0 with the applicable Jumper J8 configuration. J8 should be closed at position 2+3 in order to establish connection. Furthermore, it is also possible to connect both interrupt outputs (UART and RTC) to port 2.0 of the C167, since both have an open-drain output and the interrupt source can be determined via the corresponding status register of the chips. All signals are available via the pins to the edge of the board.

A constant voltage source of 3 - 4 V must be connected to the VBAT input (pin B20) in order to maintain data stored in the Real-Time Clock (RTC) independently from the VCC, as well as to back-up data in the first RAM bank. The current draw of the buffered devices is less than 200 μ A (typically 5 μ A.) at room temperature (20 °C).

The miniMODUL-167 is equipped with a Power-Fail mechanism, hence allowing early detection of interruptions in the power supply. The input voltage at PFI (A61) is compared with an internal 1.3 V reference voltage and - in the event of a reduction of input voltage - switches the PFO output against the GND potential. Should the battery buffer or Power-Fail mechanism not be utilized, the VBAT input (or the PFI input) must be connected to the GND.

If the WDI input is connected, then the pin at WDI must toggle at least once a second. Otherwise, the Watchdog of the MAX690 triggers a /Reset of the miniMODUL-167. Should the Watchdog not be used, then the WDI input must remain unconnected.

6 Real-Time Clock RTC-8583 (U10) or RTC-8564 (U15)

For real-time or time-driven applications, the miniMODUL-167 is equipped with an RTC-8583 or RTC-8564 Real-Time Clock at U10 or U15. This RTC device provides the following features:

- Serial input/output bus (I²C)
- Power consumption (RTC-8583/8564)
 - Bus active: max. 10 mA/50 mA
 - Bus inactive, CLKOUT = 32 kHz : max. - /3.4 μ A
 - Bus inactive, CLKOUT = 0 kHz : max. 50 μ A / 0.80 μ A
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions
- 240 byte SRAM (RTC-8583 only)

If the miniMODUL-167 is equipped with a battery, the Real-Time Clock runs independently of the board's power supply.

Programming the Real-Time Clock is done via the I²C bus (address 0xA2 = 10100010), which is connected to port P2.1 (SCL) and port P2.2 (SDA). The Real-Time Clock also provides an interrupt output that extends to port P2.0 via Jumper J8. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. An interrupt must be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. *For more information on the features of the RTC-8583/8564, refer to the corresponding Data Sheet.*

Note:

After connection of the supply voltage, or after a reset, the Real-Time Clock RTC-8583 generates an interrupt periodically. The RTC-8564 doesn't generate interrupts after connecting a supply voltage. The RTC must first be initialized (*see RTC Data Sheet for more information*).

7 Serial E²PROM/FRAM (U16)

The miniMODUL-167 is populated with a non-volatile memory with a serial interface (I²C interface) to store configuration data. According to the memory configuration of the module, an E²PROM (4 to 32 kByte) or FRAM can be mounted at U16.

A description of the I²C memory protocol of the specific memory component at U16 can be found in the respective Data Sheet.

Table 18 gives an overview of the memory components that can be used at U16 at the time of printing of this manual.

Device Type	Manufacturer	Size	Component
E ² PROM	Microchip	32 kByte	MIC24LC256
	Catalyst	4 kByte*	CAT24WC32
		8 kByte	CAT24WC64
	ST	4 kByte*	M24C32
		8 kByte	M24C64
FRAM	Ramtron	512 Byte	FM24C04
		8 kByte	FM24C64

*= Default size

Table 18: Memory Device Options for U16

Various available E²PROM/FRAM types provide a write protection function¹. Jumper J14 is used to activate this function. If this jumper is closed, then pin 7 of the serial E²PROM/FRAM is connected to VCC.

Write Protection E ² PROM/FRAM	J14
Write protection of E ² PROM/FRAM deactivated	open*
Write protection of E ² PROM/FRAM activated	closed

* = Default setting

Table 19: E²PROM/FRAM Write Protection

¹: Refer to the corresponding E²PROM/FRAM Data Sheet for more information on the write protection function.

Jumper J15 and J16 configure the address of the serial E²PROM/FRAM. The default configuration sets the address to 0xA8.

E²PROM/FRAM Address	J15	J16
0xA0	1 + 2	2 + 3
0xA4	2 + 3	2 + 3
0xA8	1 + 2*	1 + 2*
0xAC	2 + 3	1 + 2

* = Default setting

Table 20: E²PROM/FRAM Address

8 Technical Specifications

The physical dimensions of the miniMODUL-167 are represented in *Figure 7*. The module's profile about 10 mm thick, with a max. height of the components of 5 mm on the soldering-side as well as on the component-side. The board itself is approx. 1.5 mm thick.

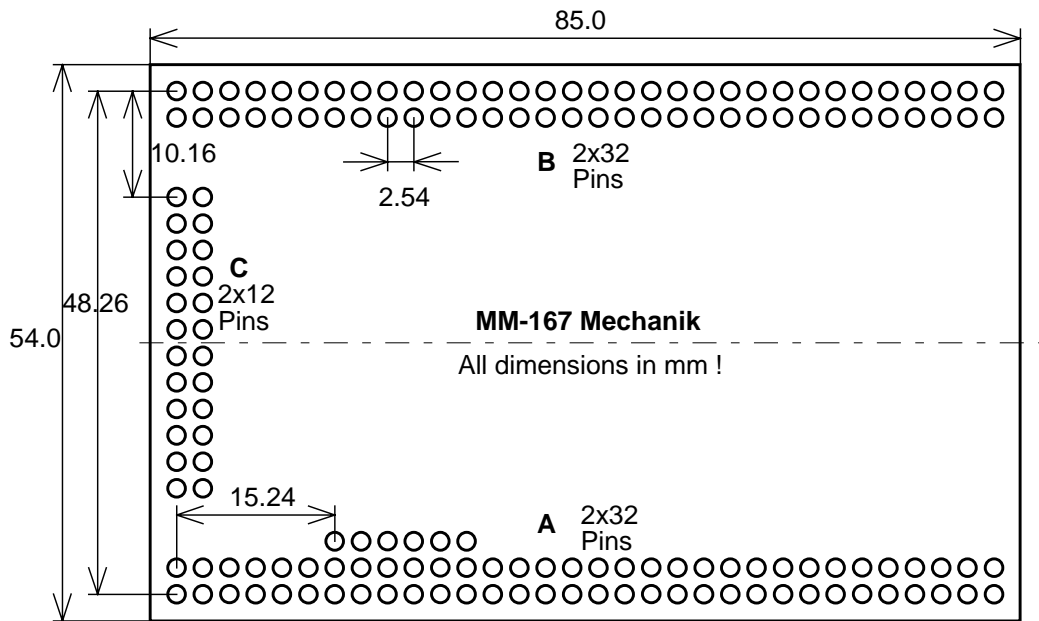


Figure 7: Physical Dimensions

Additional specifications:

- Voltage: 5 V +/- 5 %
- Power Requirements: max. 500 mA. (typ. 160 mA)
(at Ta = 20°C, Fosc = 20 MHz,
Vcc = 5 V)
- Storage Temperature: -40 to +90 °C
- Operating Temperature: 0 to +70 °C, extended: -40°C to +85°C
- Humidity (rel.): 95 % r.F. not condensed
- Dimensions.: 85 x 54 x 15 mm. (l x w x h) +/- 1 mm.
IC height above/below the board: max
5 mm.

Note:

This data specifically refers to the standard configuration of the miniMODUL-167. Its typical power requirement is lower than 160 mA (*refer to table below*).

Standard Board MM-310 with standard GAL device 16V8H-15

RUN (Monitor runs out of RAM)	155 mA
RESET	125 mA
IDLE	95 mA
POWERDOWN	55 mA

Board with zero-power GAL device 16V8Z-15

RUN (Monitor runs out of RAM)	120 mA
RESET	90 mA
IDLE	60 mA
POWERDOWN (all /CS = high)	10 – 15 mA depending on the RS-232 driver
POWERDOWN (without RS-232)	1 – 2 mA

Note:

Take precautions to adhere to ESD recommendations when handling the minMODUL's CMOS components.

Document: miniMODUL-167
Document number: L-625e_3, March 2003

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Did you find any mistakes in this manual? _____ page

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