

# Implemented improvement on the phyCORE-i.MX 6 SOM (PCM-058 and PCL-058) related to sporadic display freezing

The information in this document is relevant to the phyCORE-i.MX 6 System on Module with product numbers PCM-058 and PCL-058, as well as corresponding SBCs with the product number PB-01501.

## Issue:

In rare cases the system can fall into a freezing state when the CPU is operating with low frequency and there is load on the VPU. This was seen in combination with an LVDS display. This issue is caused by a small voltage drop, internal to the i.MX 6, from VDD\_MX6\_SOC to VDDSOC\_CAP (voltage domain).

## Workaround:

The system stability can be improved by increasing the VDD\_MX6\_SOC domain to 1.25V for low frequencies.

Moreover, when using any BSP version PD16.1.x, the LDO\_PU path should be set to bypass mode. This change is already implemented in 18.1.x.

We recommend updating currently stocked units and any future systems with a new Linux Kernel containing the patches listed below.

## Available Linux patches:

The Linux implementation can be found in the corresponding *git* repositories:

<https://git.phytec.de/linux-mainline/commit/?h=v4.1.46-phy&id=4852bf82897726228ac54b73a266b0c9795b4d24>

<https://git.phytec.de/linux-mainline/commit/?h=v4.1.46-phy&id=3f55a7401f32fdb5e4992fd78ccde633491cf76f>

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